

Compal Confidential

MB Schematic Document

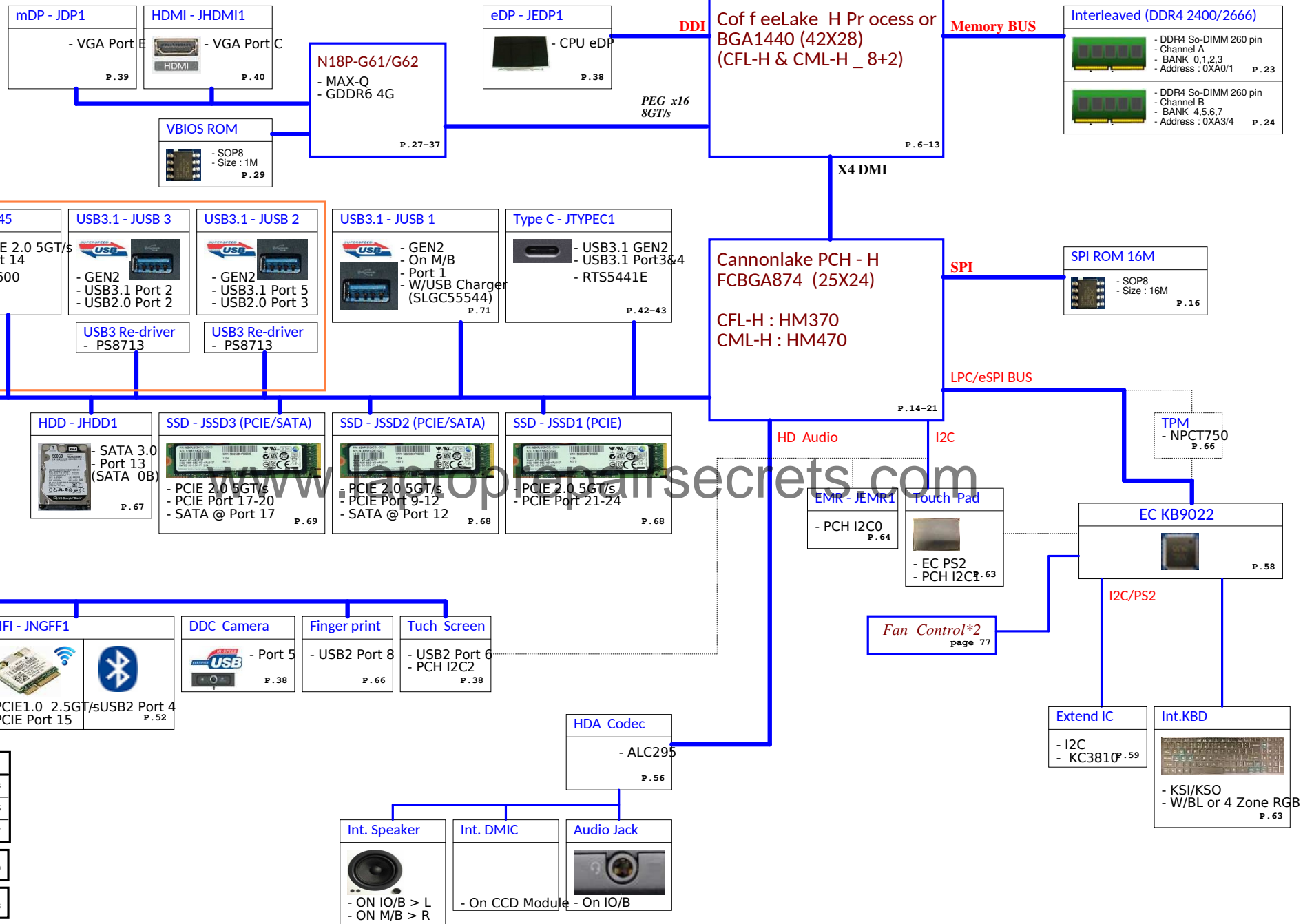
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FH51M LA-J871P

Rev:1.0

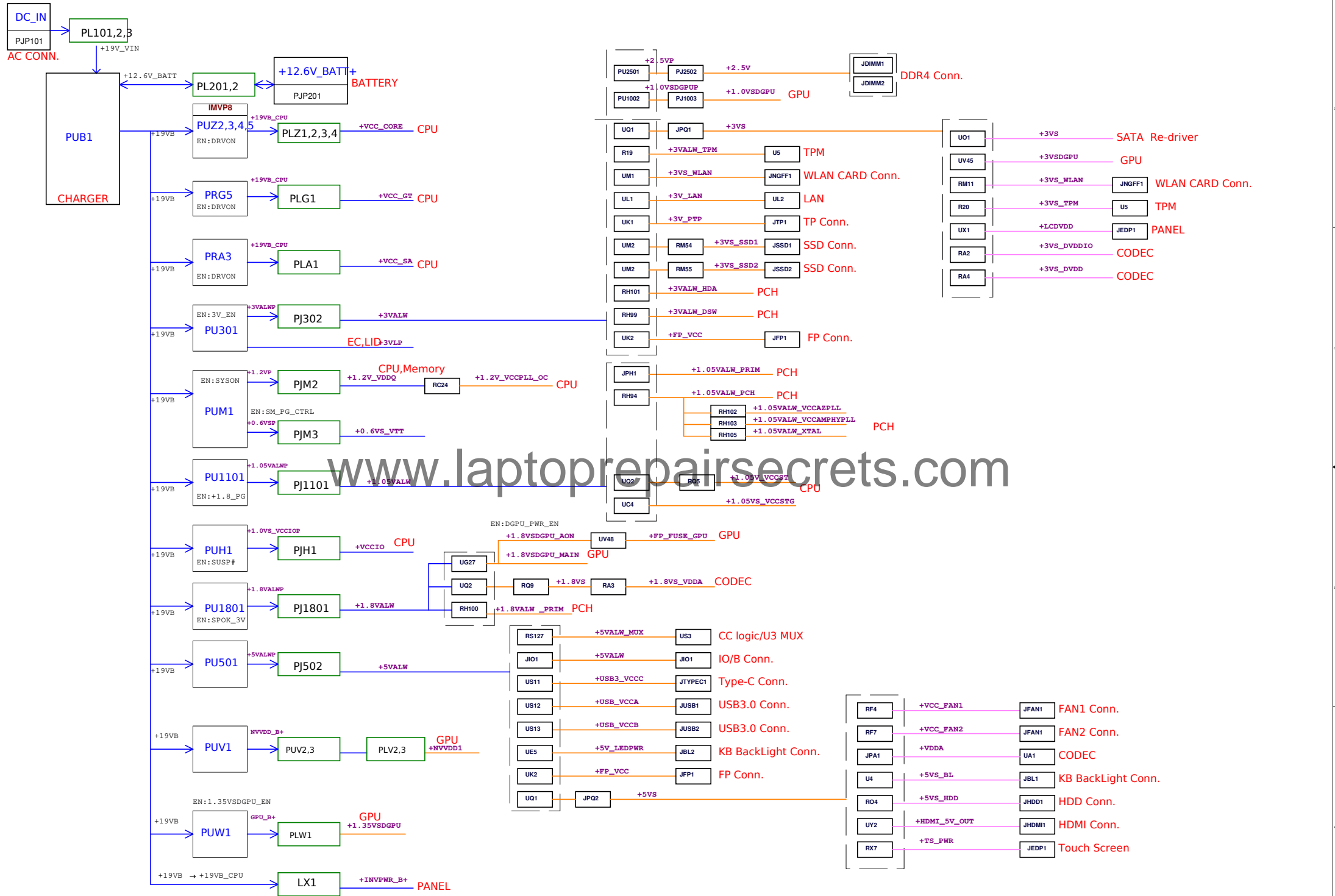
2020.02.11

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Sub Board	
IO/B (JIO1/JIO2)	P. 73
HS/B (JHS1)	P. 66
TURBO/B (JTURBO1)	P. 77
RTC CKT. (JRTC1)	P. 20
Power On/Off CKT.	P. 63
HW Circuit DC/DC	P. 78
Power Circuit DC/DC	P. 82-111

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Coffee Lake-H
- Re-fresh R0 stepping

UC1
CFLI5QS@
S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00

UC5
CFLI5@
S IC CL8068404121905 SRF6X U0 2.4G
SA0000COG40

UH1
CFLPCHOS@
S IC FH82HM370 QNYF B0 BGA 874P PCH-
SA0000BPF10

Comet Lake-H

UC1
CMLI5QS@
S IC CL8070104398806 QTJ1 R0 2.1G 1440 S
SA0000D3I10

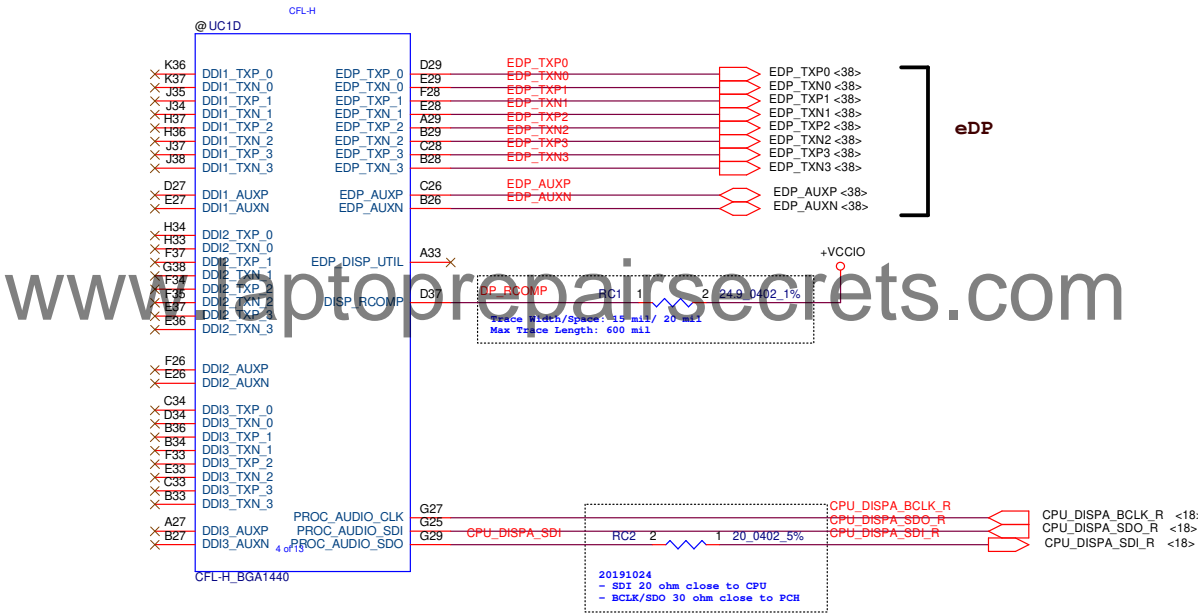
UC6
CMLI5@
S IC CL8070104399510 SRH84 R1 2.5G
SA0000DCP40

UC1
CMLI7QS@
S IC CL8070104398908 QTJ2 R0 2.4G 1440 S
SA0000D3N10

UC8
CMLI7@
S IC CL8070104399510 SRH84 R1 2.5G
SA0000DCP40

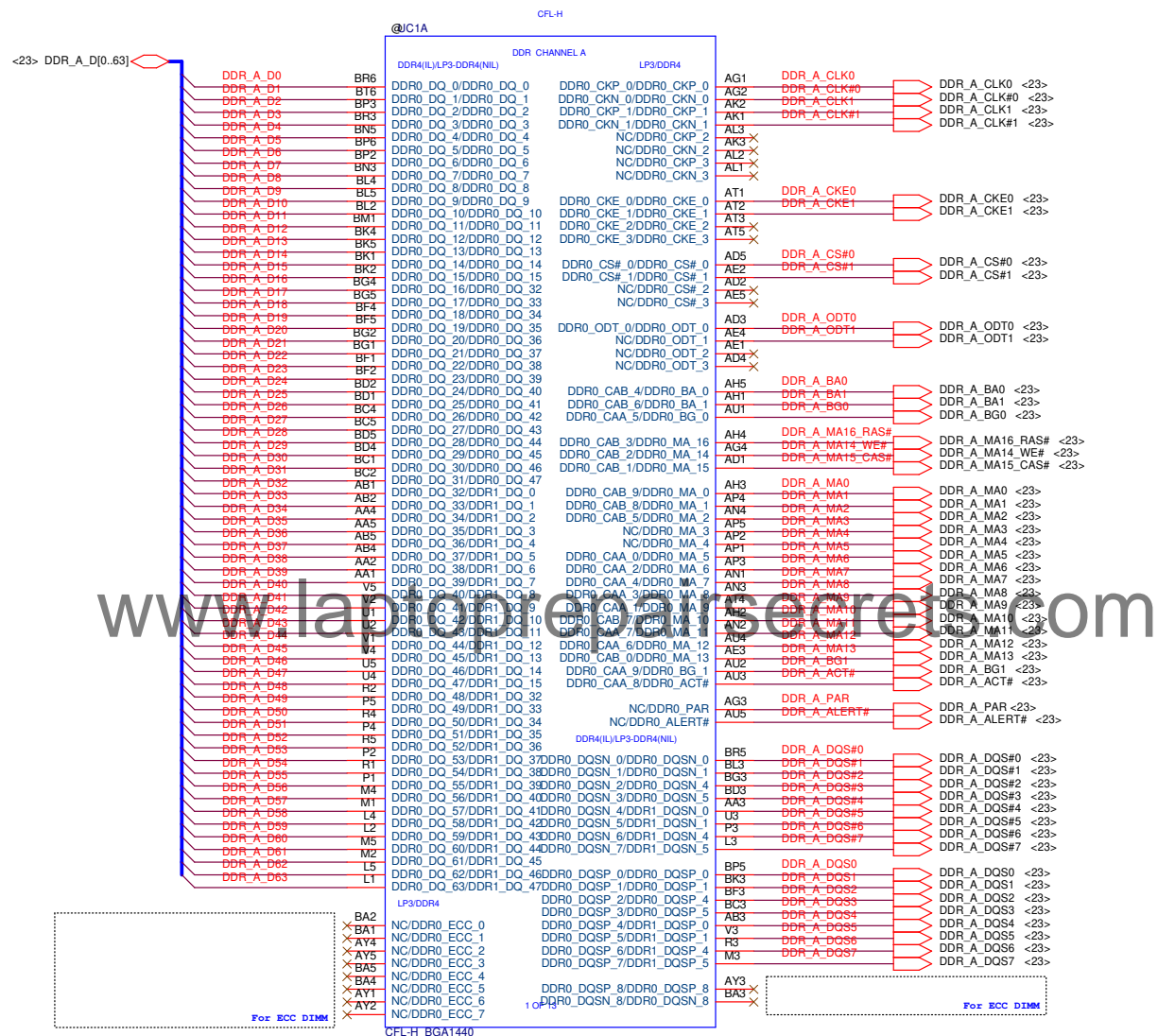
UC1
CMLI9QS@
S IC CL8070104399007 QTJ0 R0 2.8G S
SA0000D3G10

UH1
CMLPCH@
S IC FH82HM470 SRJAU A0 FCBGA PCH-H
SA0000DDP80

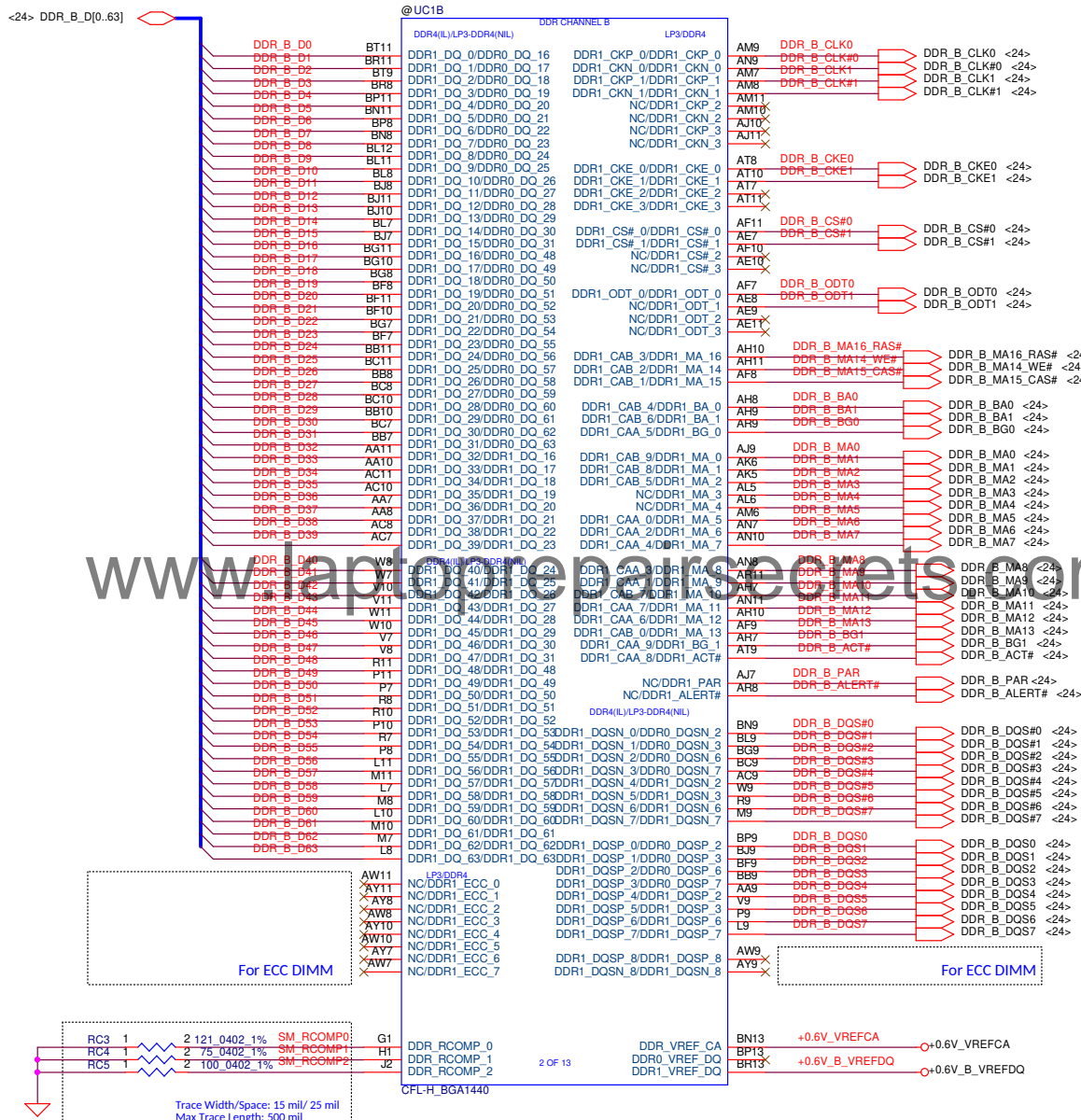


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CHANNEL-A Interleaved Memory



CHANNEL-B Interleaved Memory



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PEG&DMI

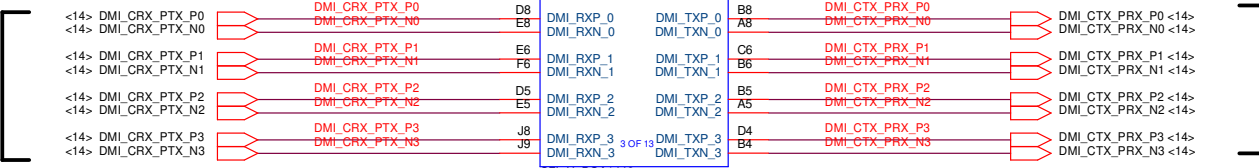
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



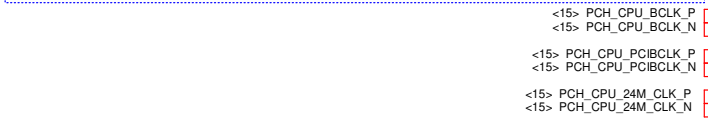
To PCH

To PCH

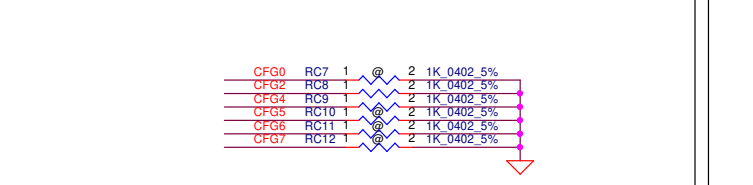
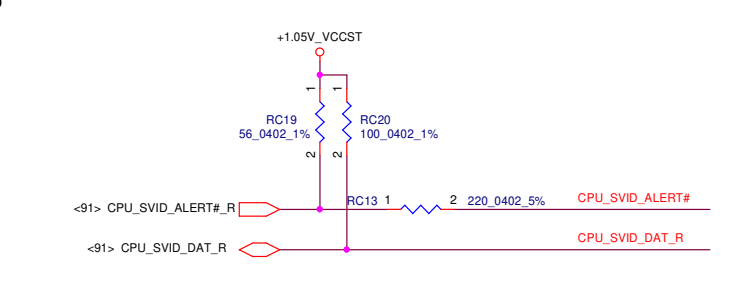
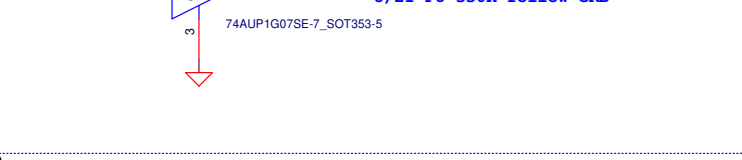
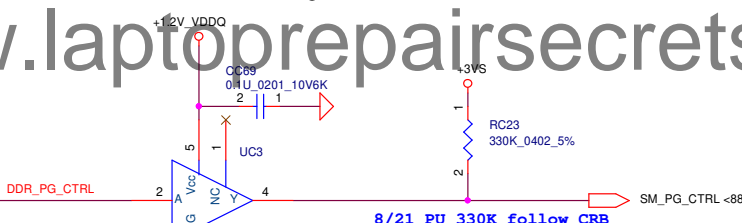
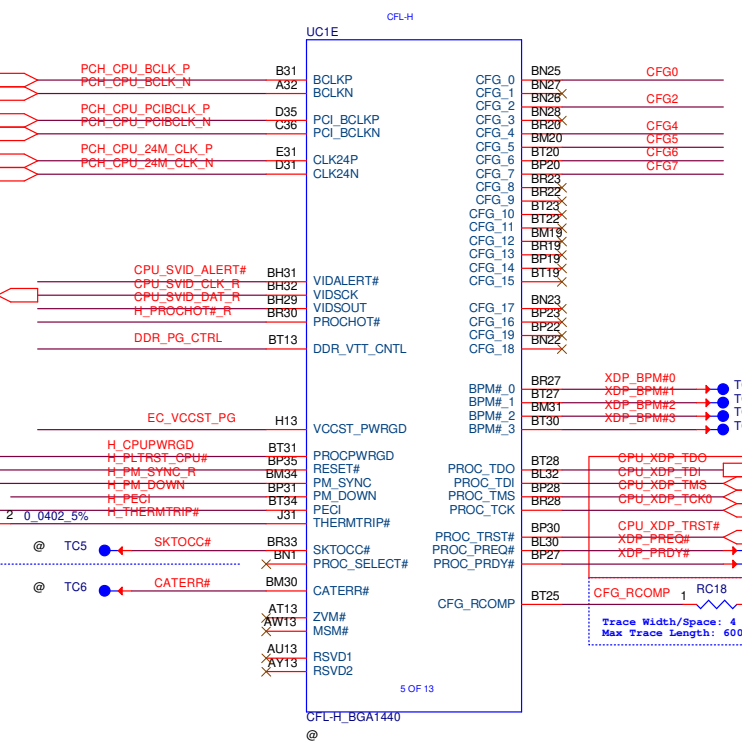
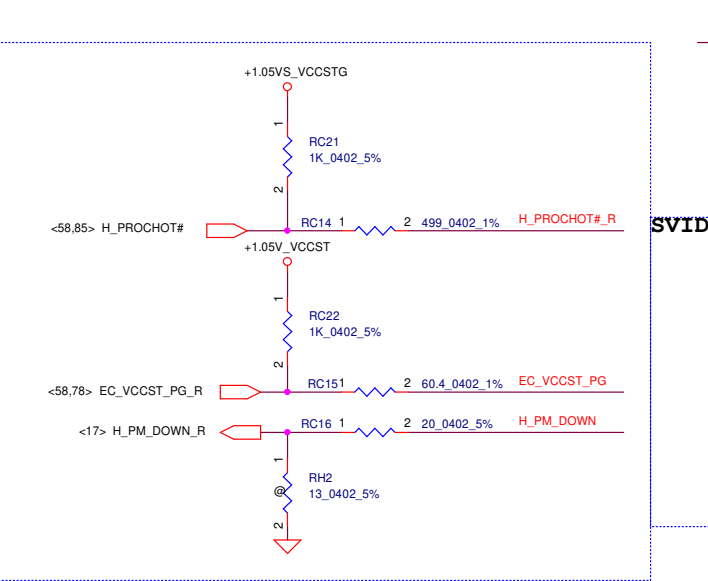
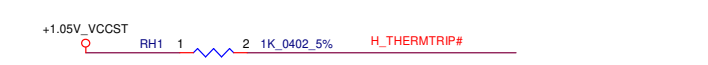
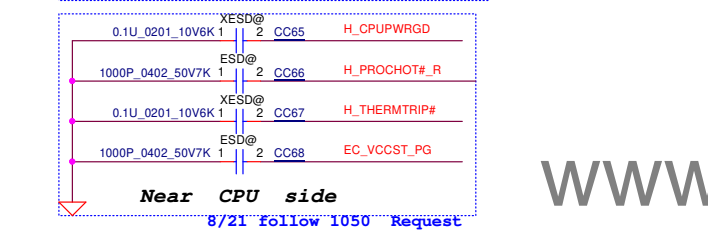


571391_CFL_H_PDG_Rev0p5

1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch) .
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.



20191024
PROC_SELECT#
> should be unconnected on CFL/CML processor



The CFG signals have a default value of '1' if not terminated on the board.

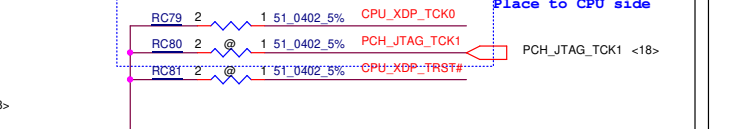
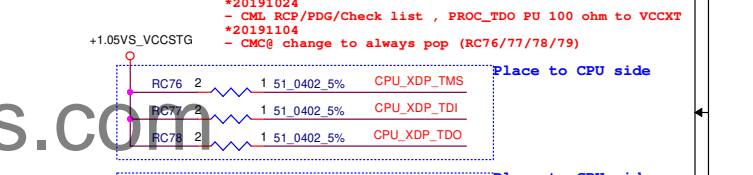
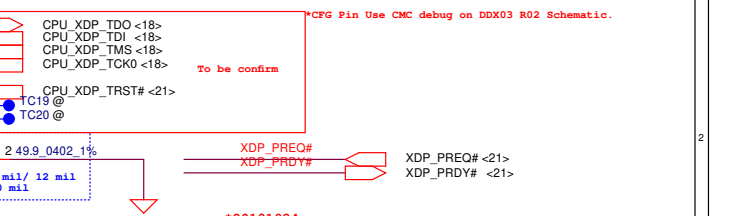
CFG[0]: Stall Reset sequence after PCU PLL lock until de-asserted
1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.

CFG[4]: aDP enable:
1 = Disabled.
0 = Enabled.

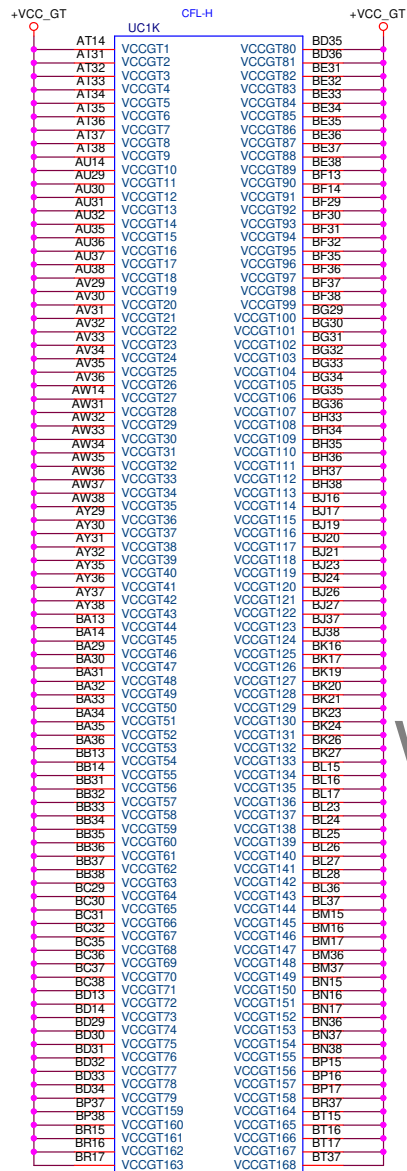
CFG[6]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
1 = (default) PEG Train immediately following RESET# de-assertion.
0 = PEG Wait for BIOS for training.



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Rev				1.0							

GT
32000mA (Hexa Core GT2)



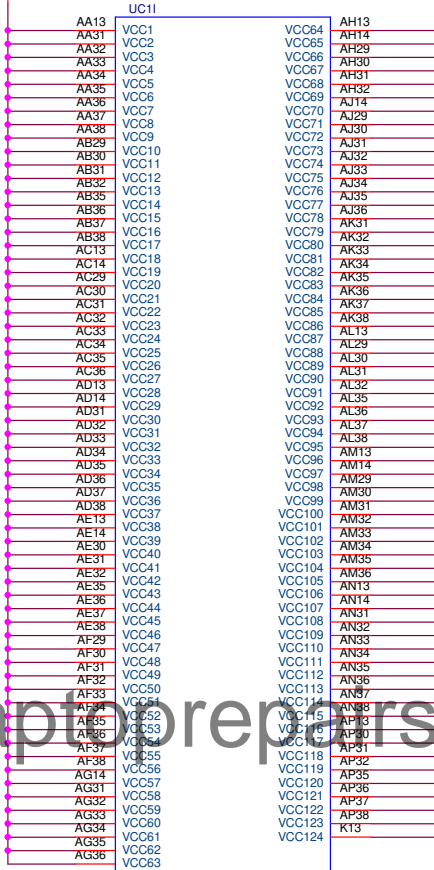
CFL-H_BGAT440
11 OF 13
VSSGT_SENSE
VCCGT_SENSE

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

+VCC_CORE

CFL-H

+VCC_CORE



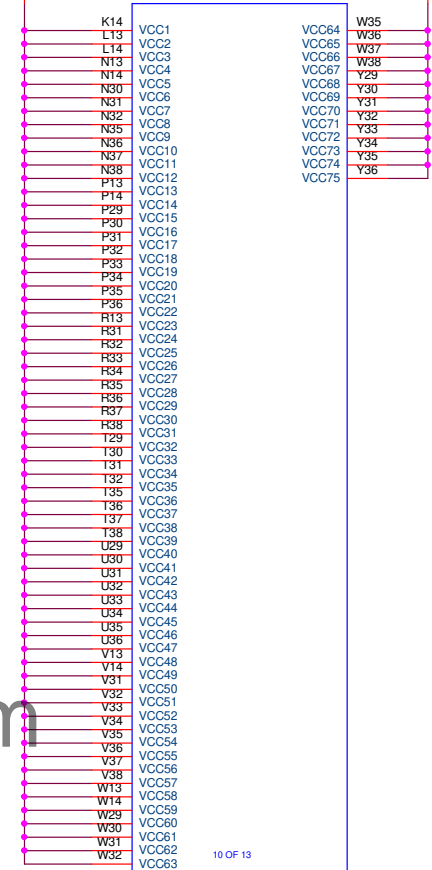
CFL-H_BGAT440
9 OF 13
VCC_SENSE
VSS_SENSE

1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

+VCC_CORE

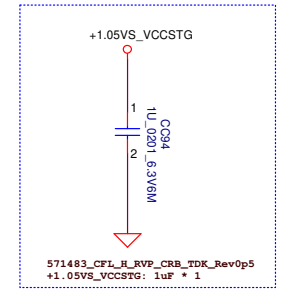
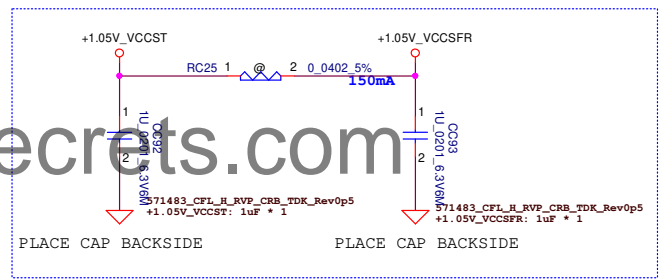
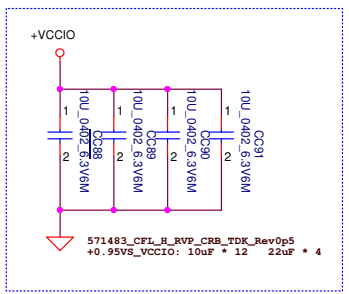
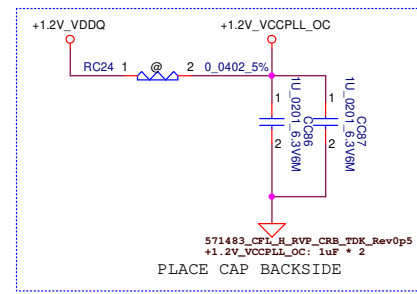
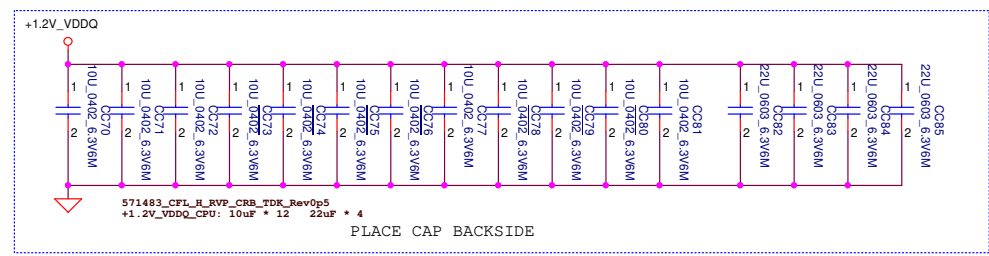
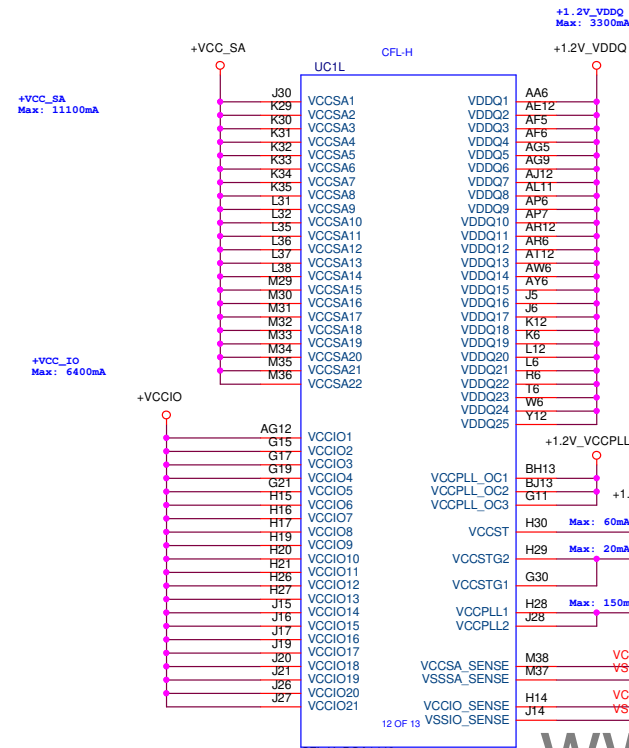
CFL-H

+VCC_CORE



CFL-H_BGAT440
10 OF 13
VCC1
VCC2

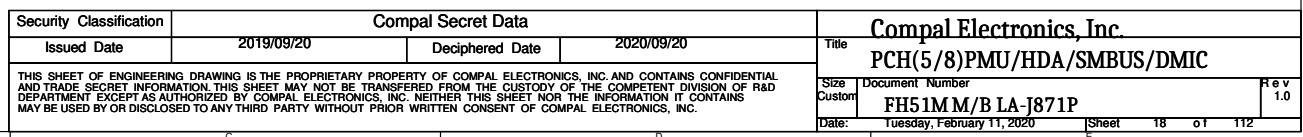
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								CFL-H(6/8)VCC CORE/GT				
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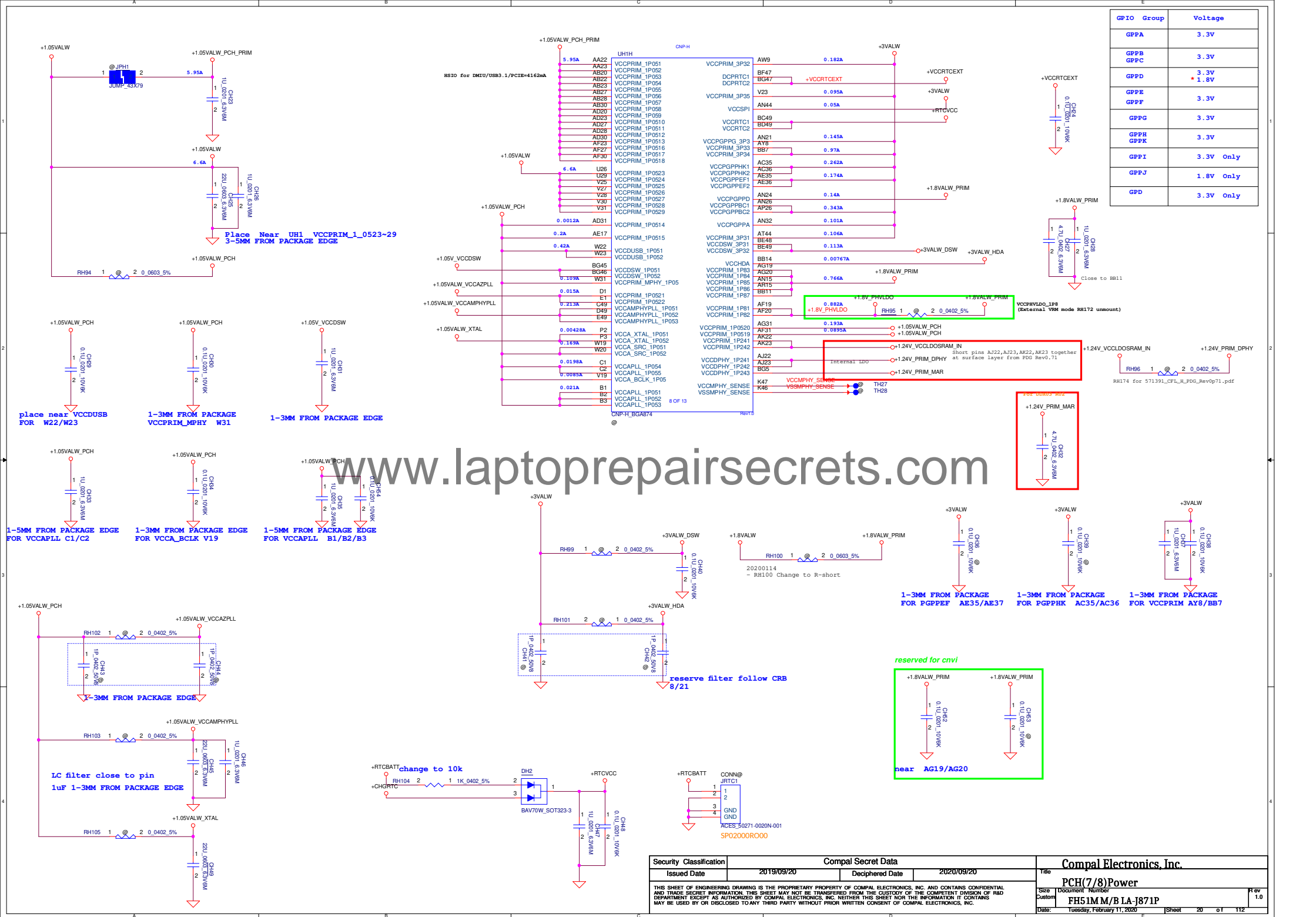


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1. VCCST_SENSE VCCST_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

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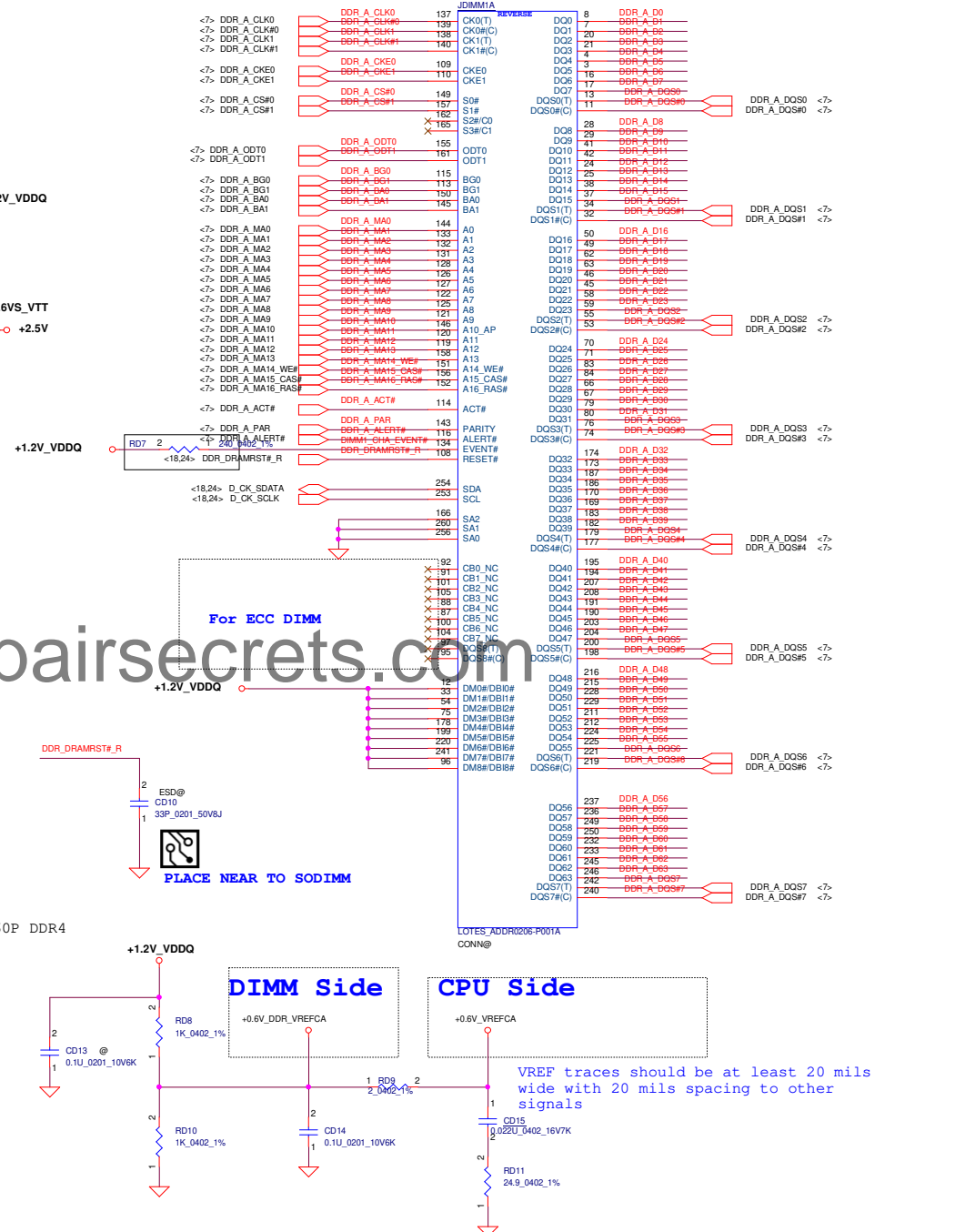
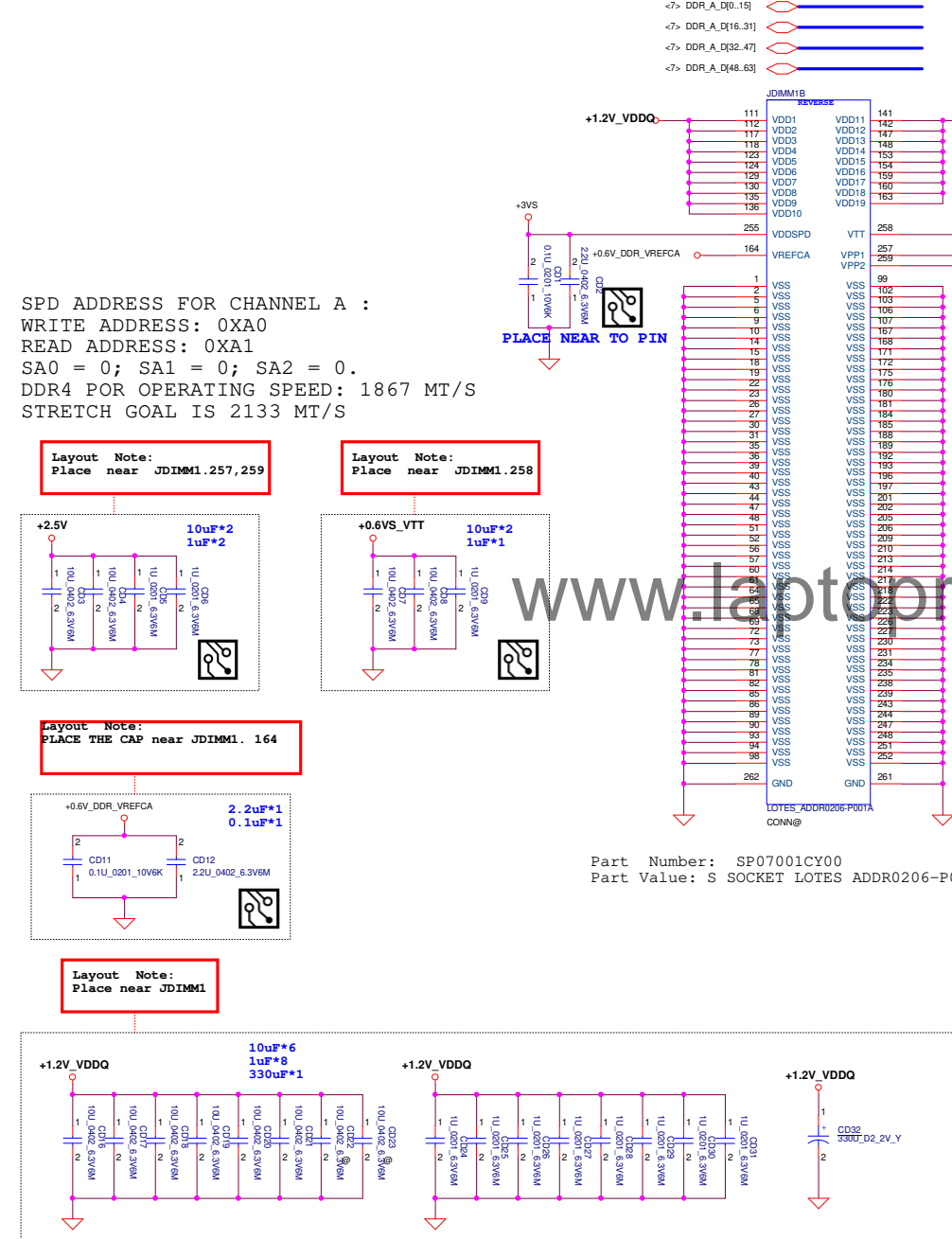




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CHANNEL-A (Interleaved Memory)

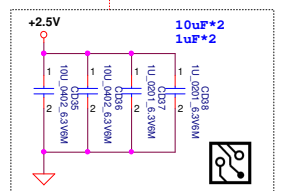
- > BOT : Reverse type (4mm)
- > Non-ECC SO-DIMM



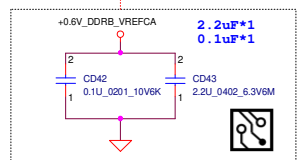
CHANNEL-B (Interleaved Memory)
> BOT : STD type (4mm)
> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

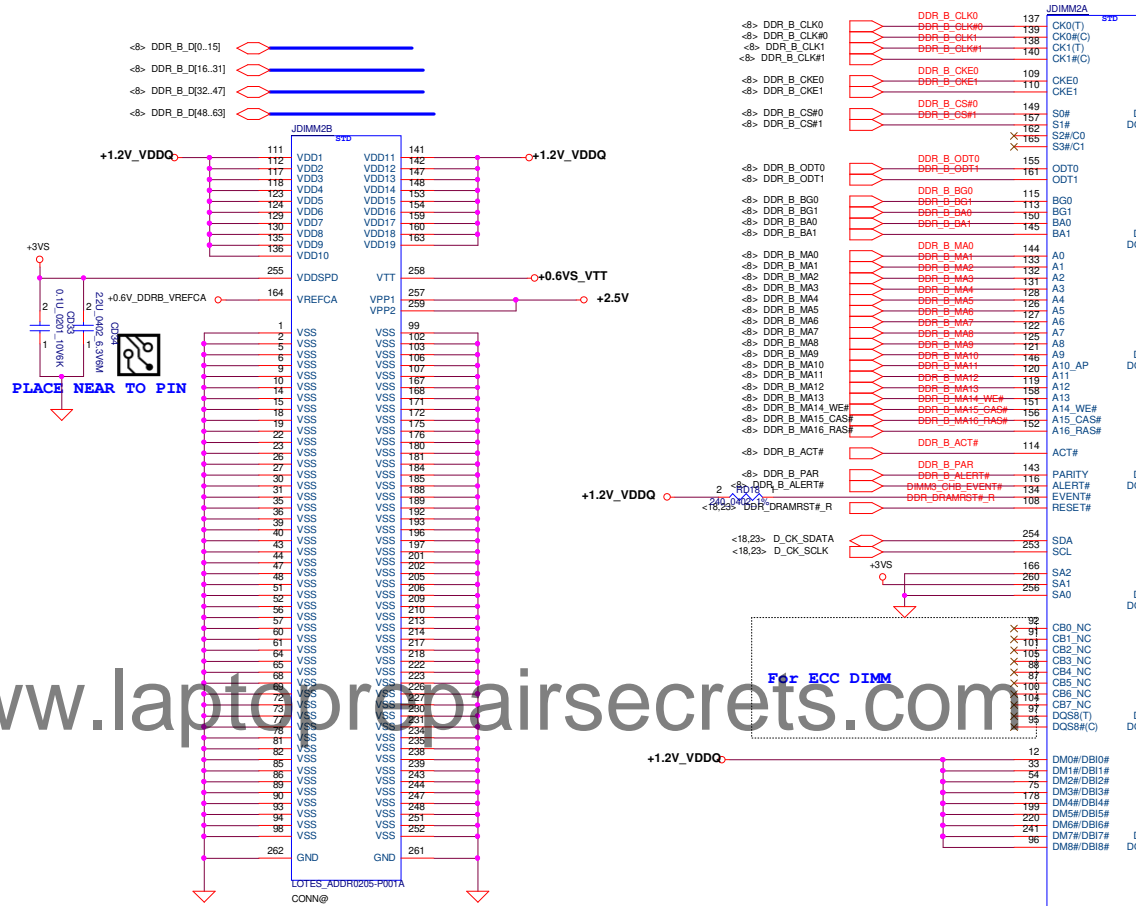
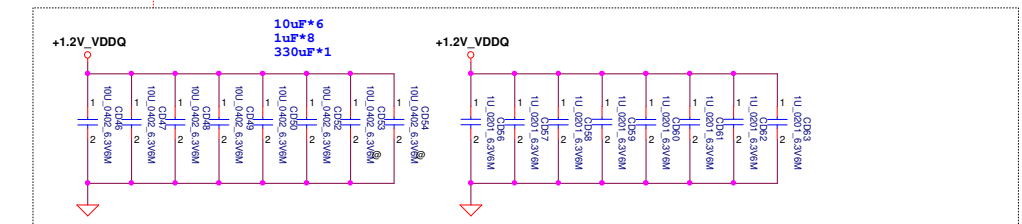
Layout Note:
Place near JDIMM3.257,259



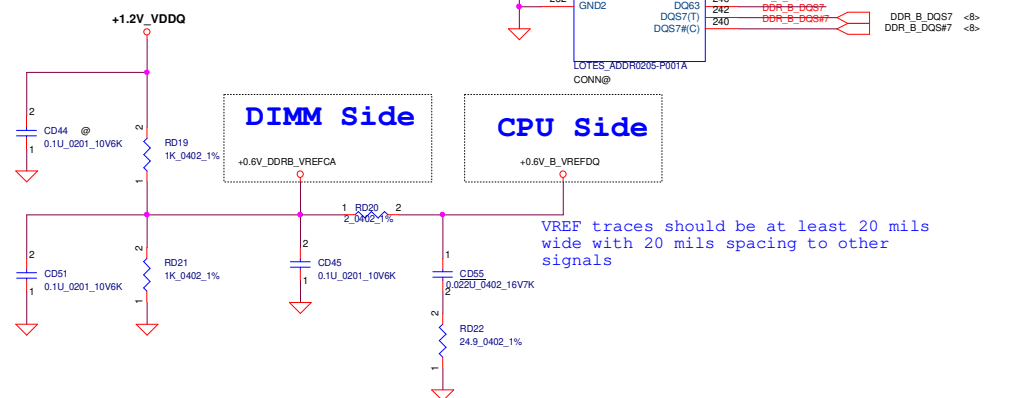
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM3



Layout Note:
Place near JDIMM3



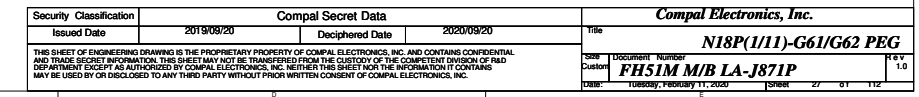
Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD

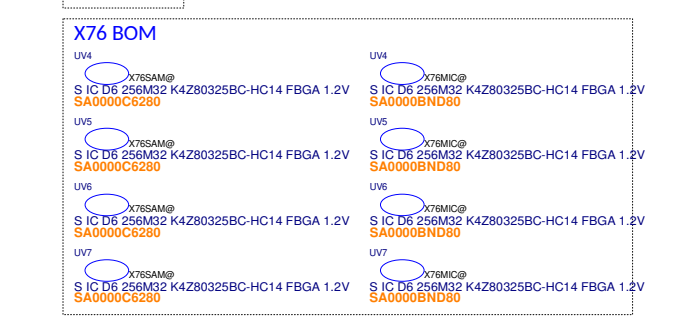
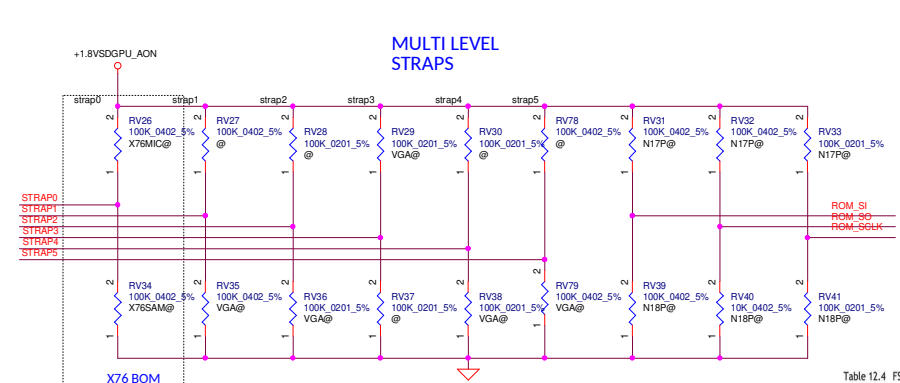
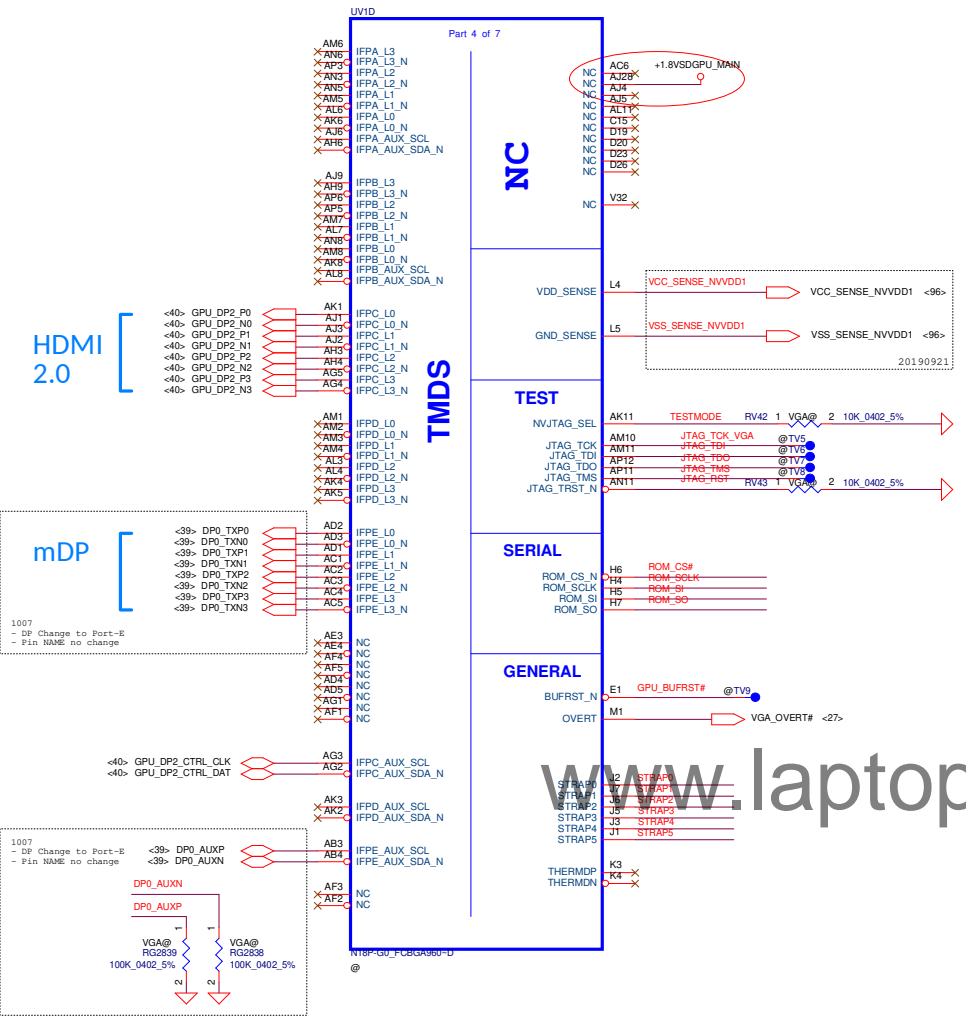


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						Sheet 24 of 112		

UV1
[redacted] VGAG61@
S IC N18P-G61-MP2-A1 BGA 960P GPU
SA0000CZO50

UV1
[redacted] VGAG62@
S IC N18P-G62-A1 BGA 960P GPU
SA0000CZP30





Strap Pins see Note 1				FS_OVERT* Function	
ROM_SO	ROM_SI	ROM_SCLK		FS_OVERT* Function	
L	L	L	L	FS_OVERT* Function ENABLED	
L	L	L	H	FS_OVERT* Function DISABLED	(Reserved; do not configure)
all other configuration				Invalid; do not configure	

Table 8. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDP0	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Cx256Mx16	1.2V	Micron	MT61K256M32E-14:A	A-die	0x1	14 Gbps	1940 ³	Full	Production candidate
		1.25V ²	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ⁴	Full	Production candidate

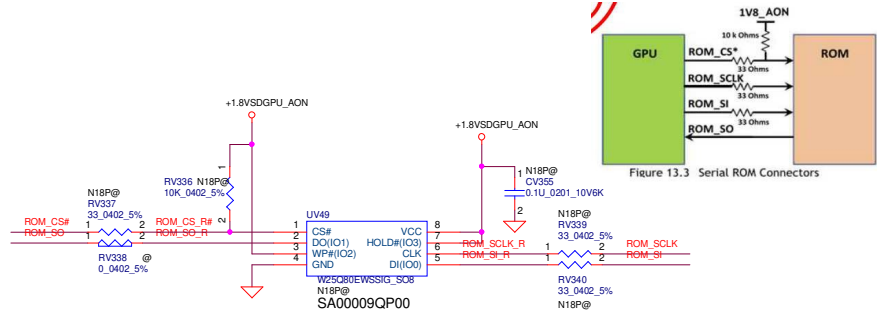
Notes:

- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- DVS is required to run WCLK > 5500 MHz.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.

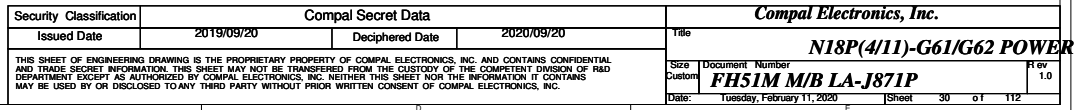
Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

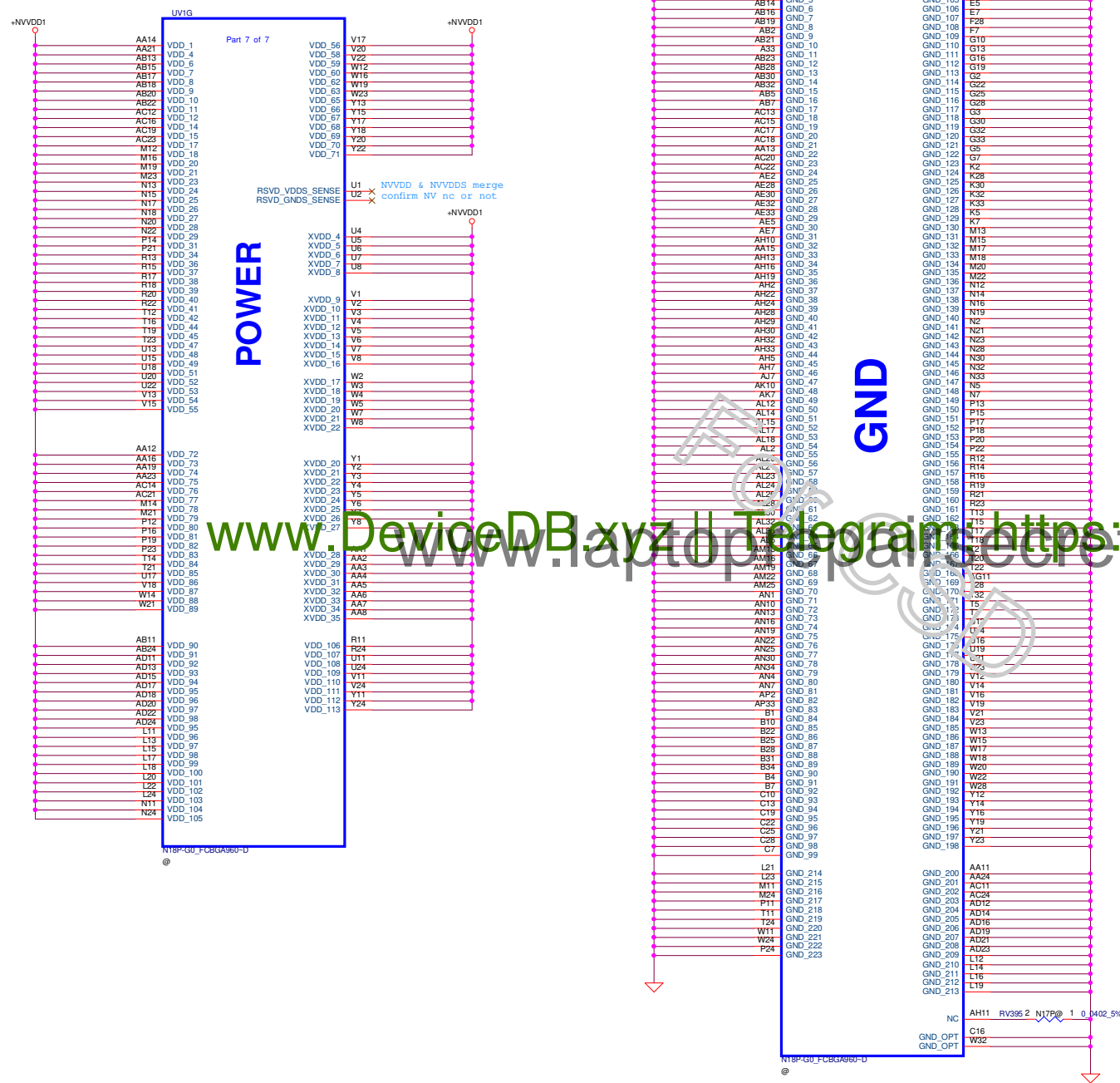
Strap Pins Note 1		Functions Selected by This Strapping				
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	0
L	H	L	0	0	1	1
L	H	H	0	1	0	1
H	L	L	0	1	0	0
H	L	H	0	1	1	1
H	H	L	0	0	0	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	0	0	0
M	L	H	1	0	1	0
M	H	L	1	1	1	0
M	H	H	1	1	1	1



SMB_ATI_ADDR	
Low	Single GPU
High	Dual GPU
DEVID_SEL	
Low	Orig. Device ID
High	Support G-Sync GPUID
VGA_DEVICE	
Low	3D Device
High	VGA Device
PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude



N17P VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2

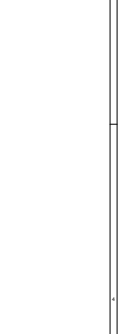
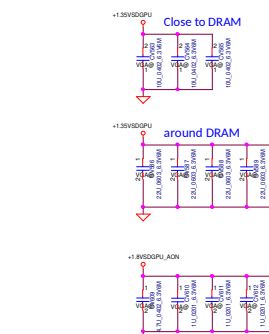
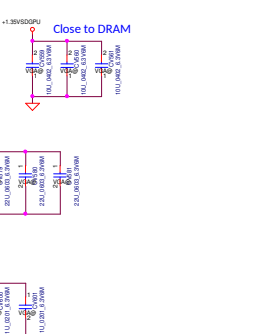
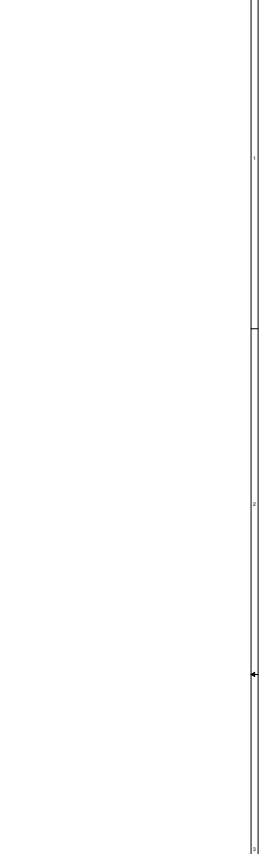
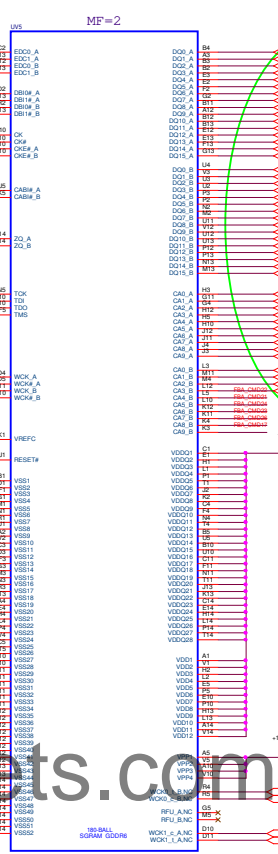
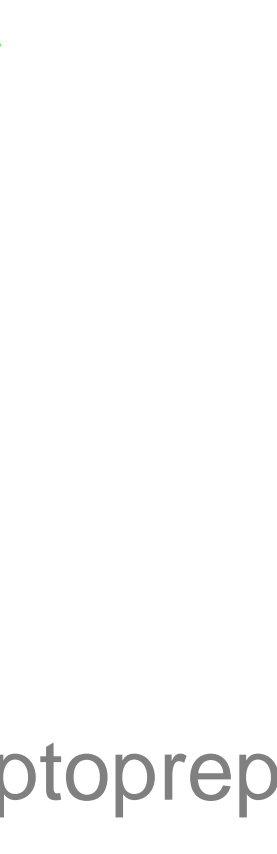


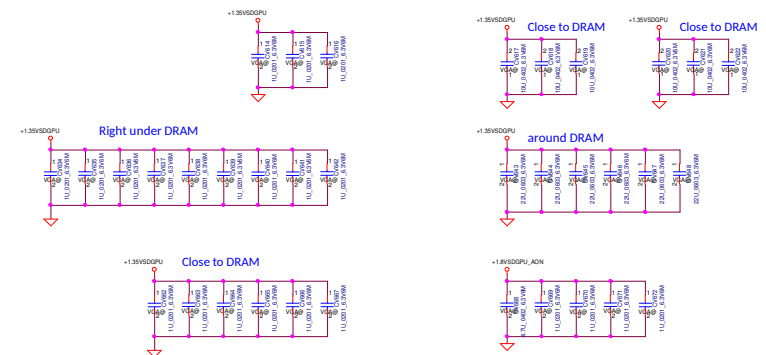
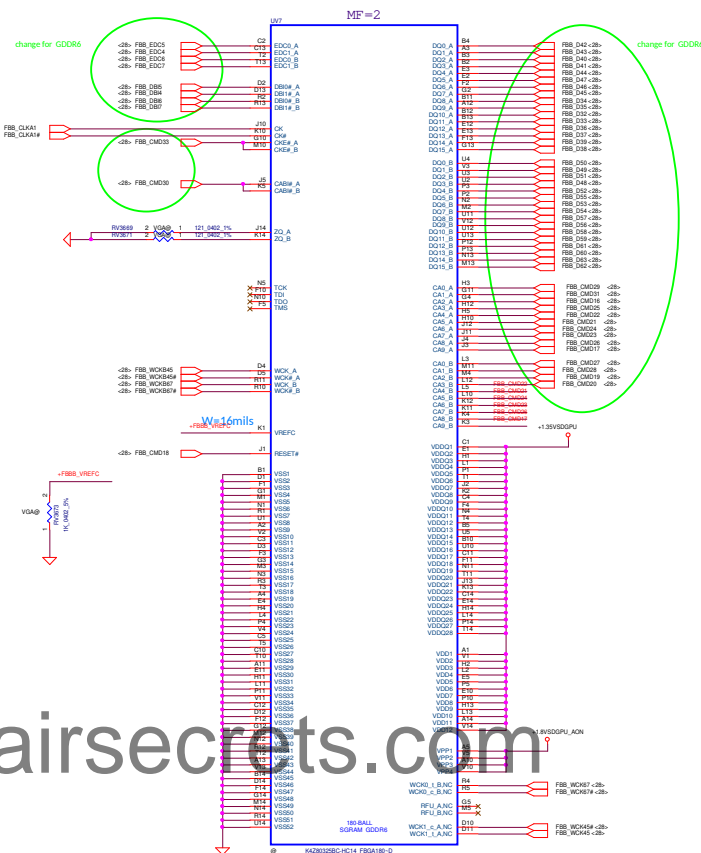
Part 6 of 7

GND

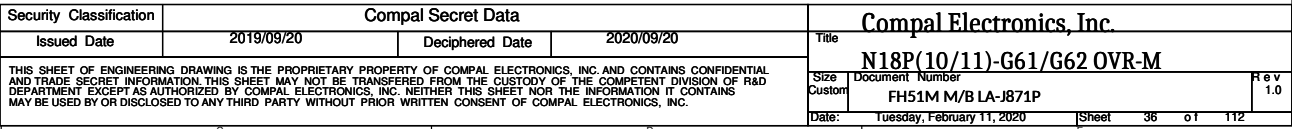
www.DeviceDB.xyz || Telegram: https://t.me/DeviceDB

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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	N18P(5/11)-G61/G62 POWER & GND
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Size	Document Number	Rev			
Custom	FH51M M/B LA-J871P	1.0			
Date:	Tuesday, February 11, 2020	Sheet	31	of	112

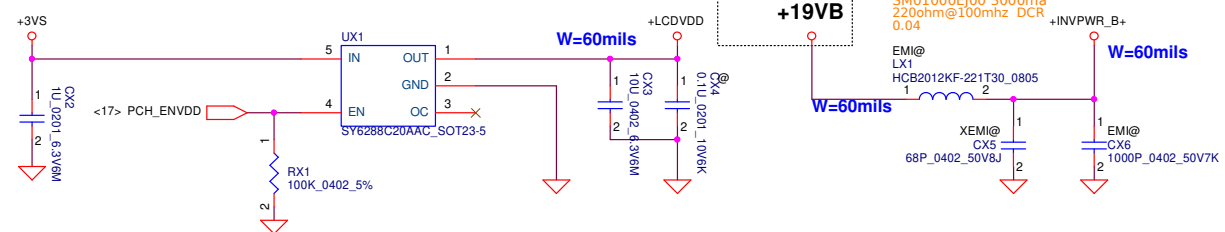




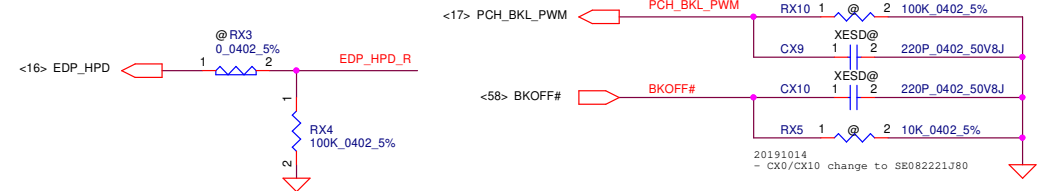
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Issued Date	2019/09/20	Declassified Date	2020/03/20	1a
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<p>USDA License Number: F5131 M/L LA-7817P</p>			<p>1.0</p>	



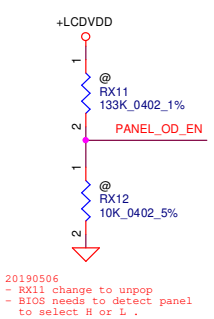
LCD POWER CIRCUIT



LCD enable signal

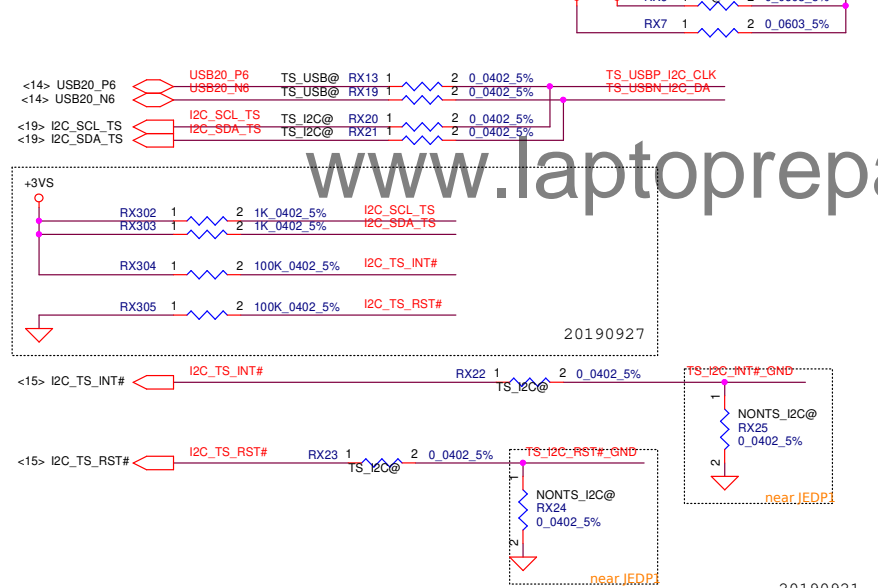


Panel OD

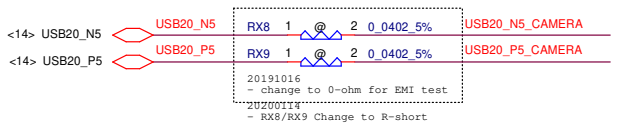


20190506
- RX11 change to unpop
- BIOS needs to detect panel
to select H or L.

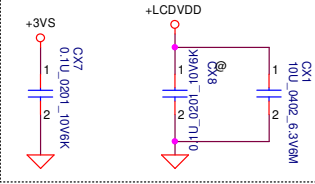
USB/I2C Touch Screen Co-Lay



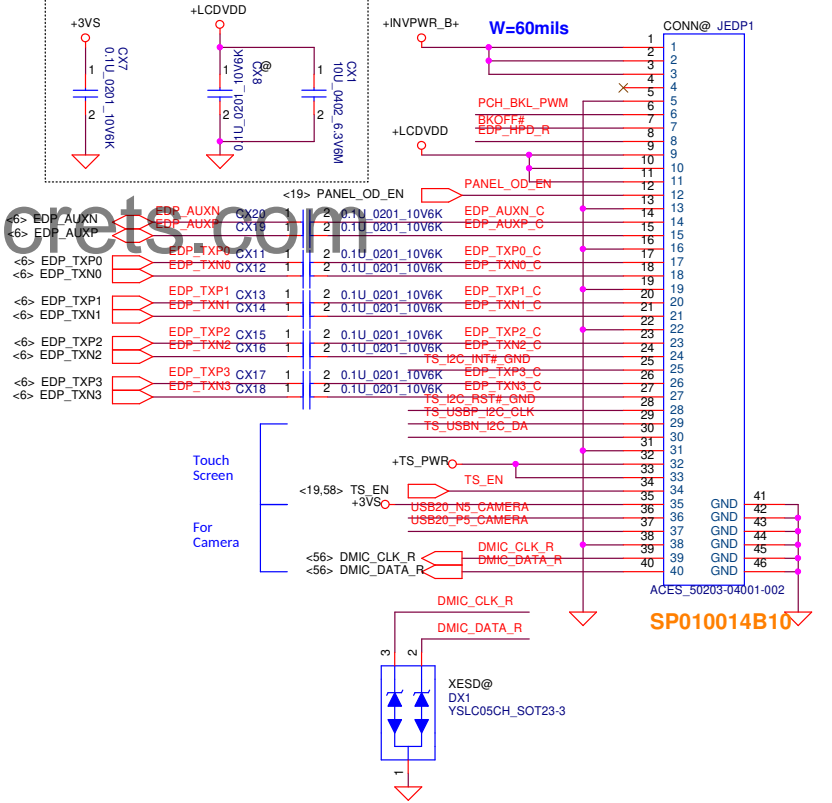
CAMERA



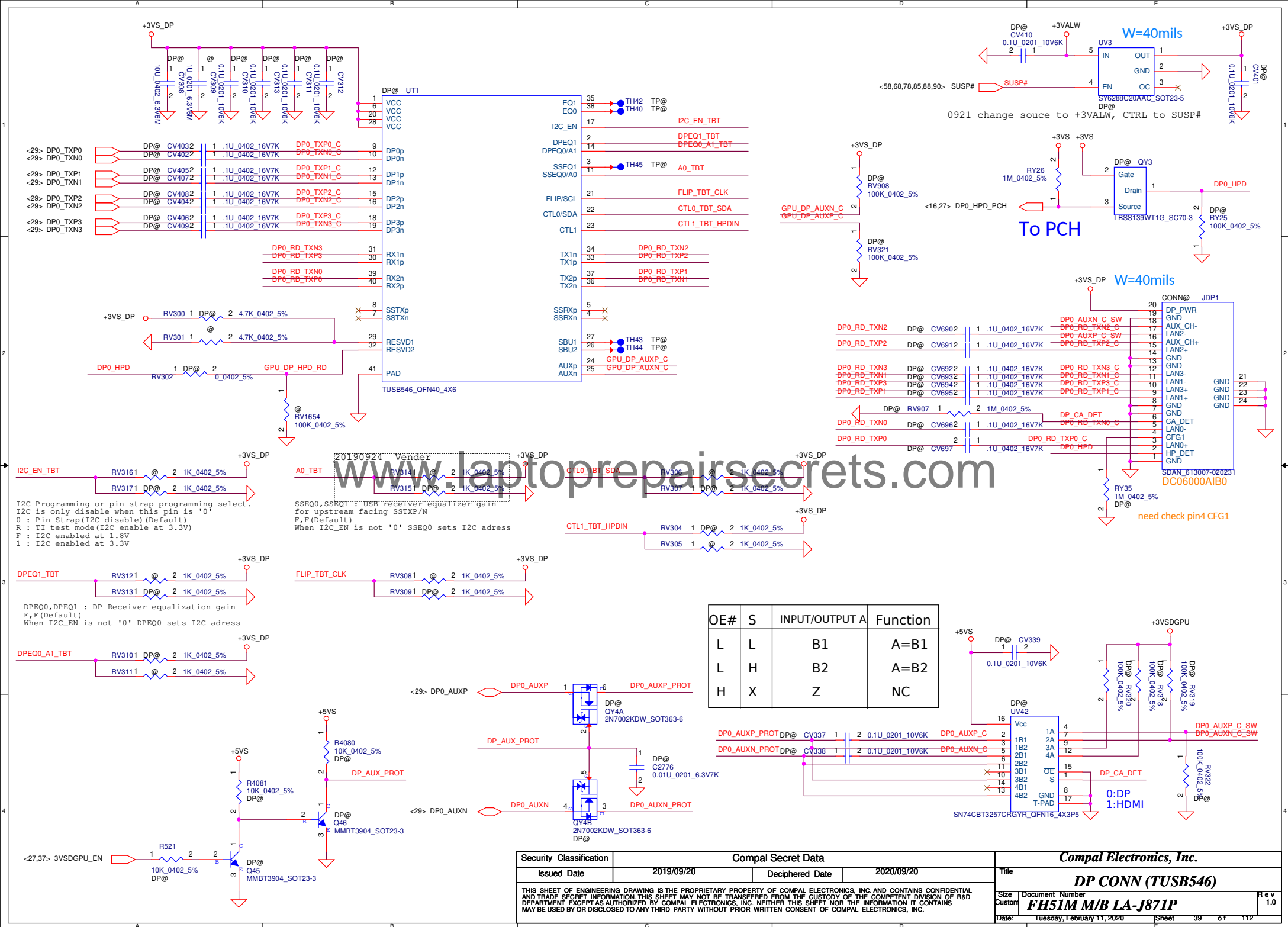
Place closed to JEDP1

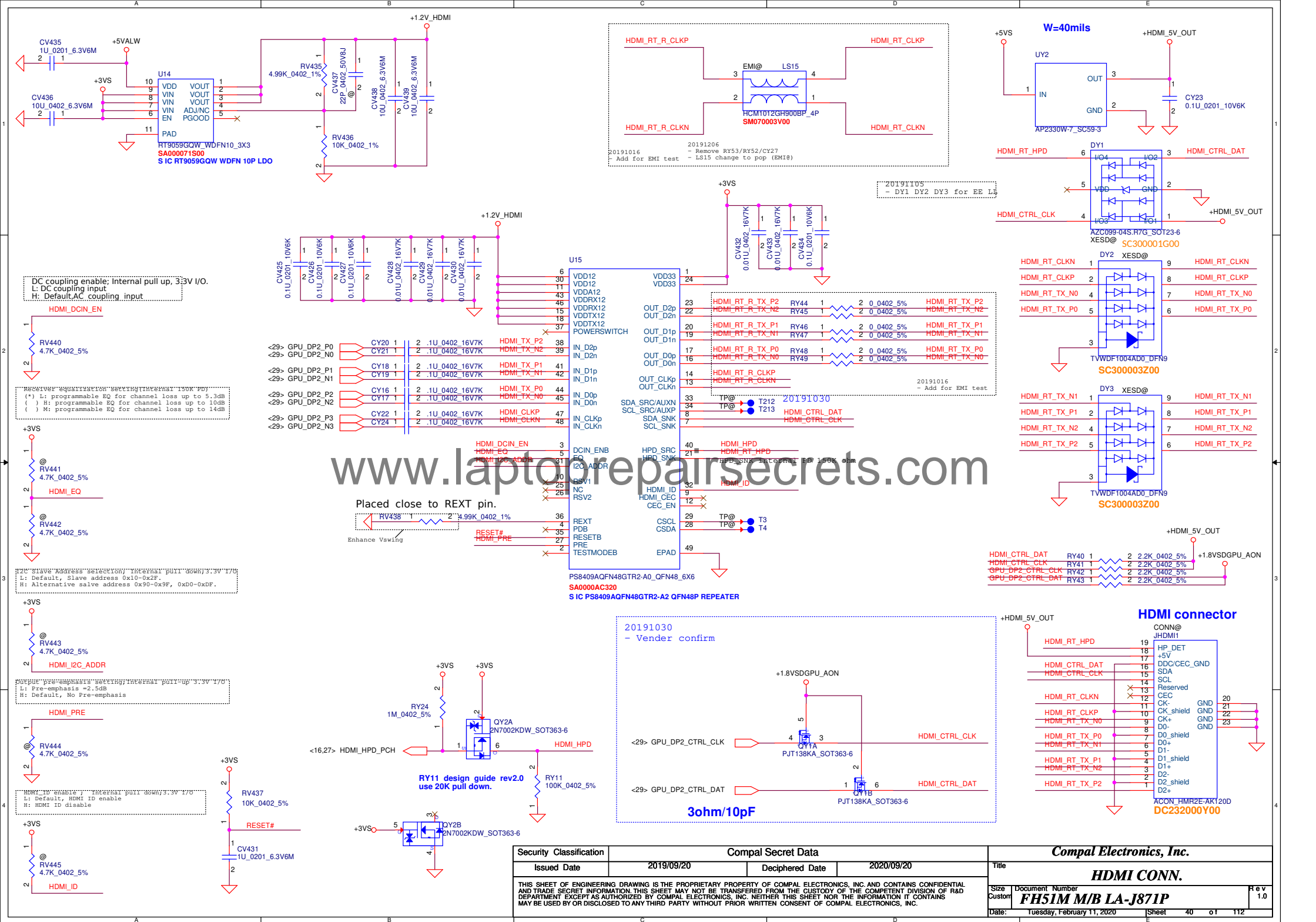


LED PANEL Conn.



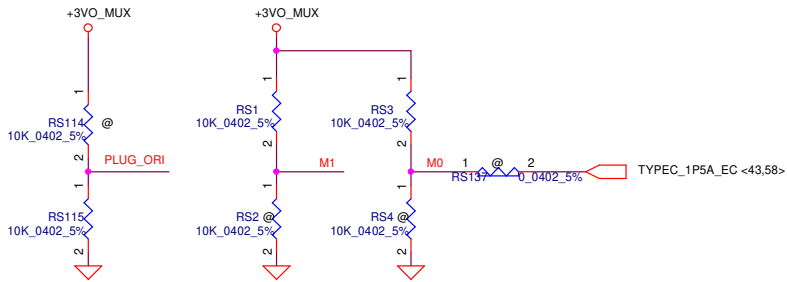
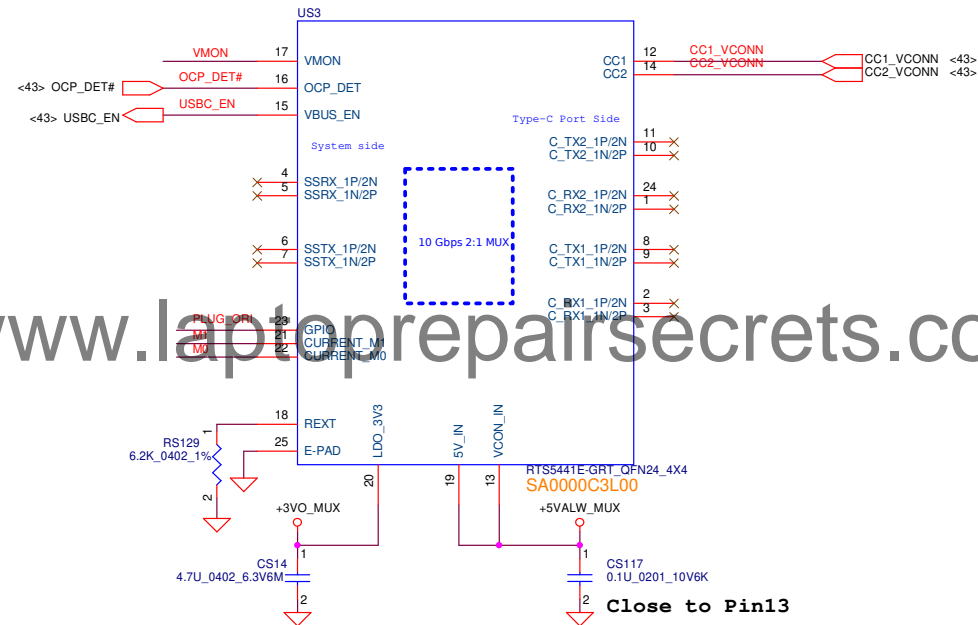
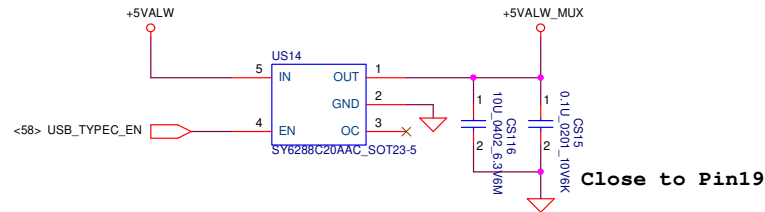
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						Size Custom		Document Number	
						FH51M M/B LA-J871P			
Date:		Tuesday, February 11, 2020		Sheet		38 of		112	





20191014

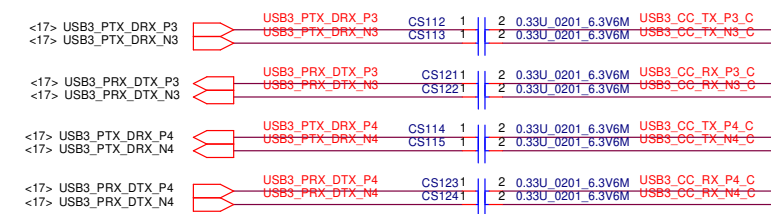
- Change to "with no Dual Role support"
- 5441E only uses the function of CC & Power SW



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

confirm realtek hand-shake			
RTS5441E M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

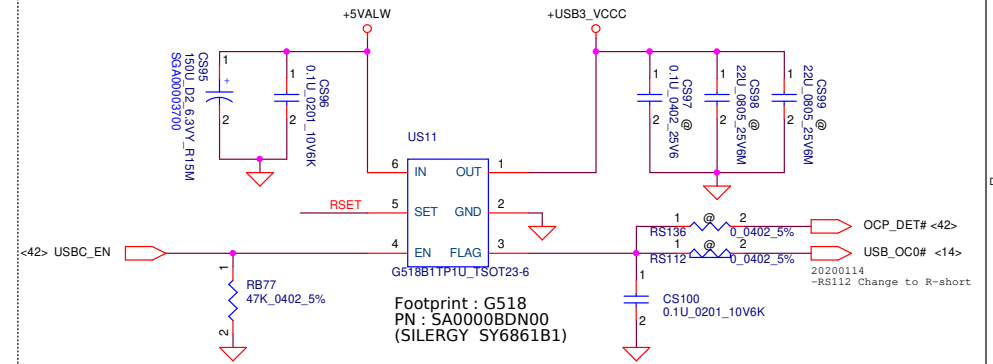
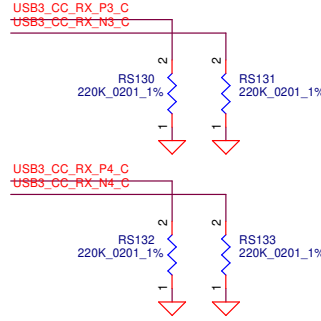
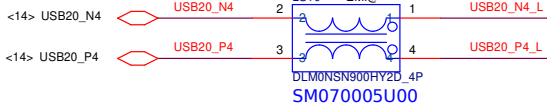
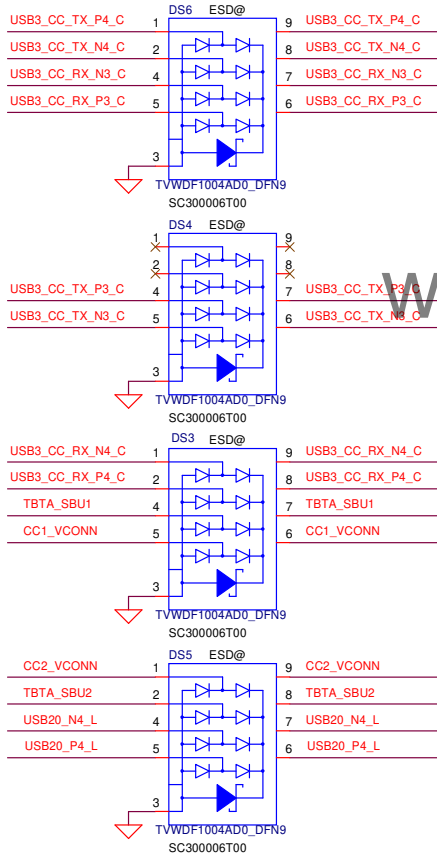
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				Sheet	42 of 112
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				Rev 1.0	



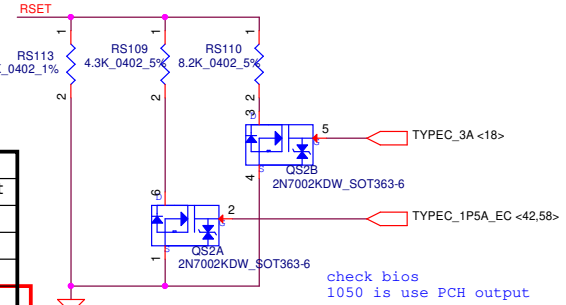
20191014
- Change to "with no Dual Role support"
- CS112/113/114/115 change to 0.33U

20191016
- USB3 Port5 change to Port3

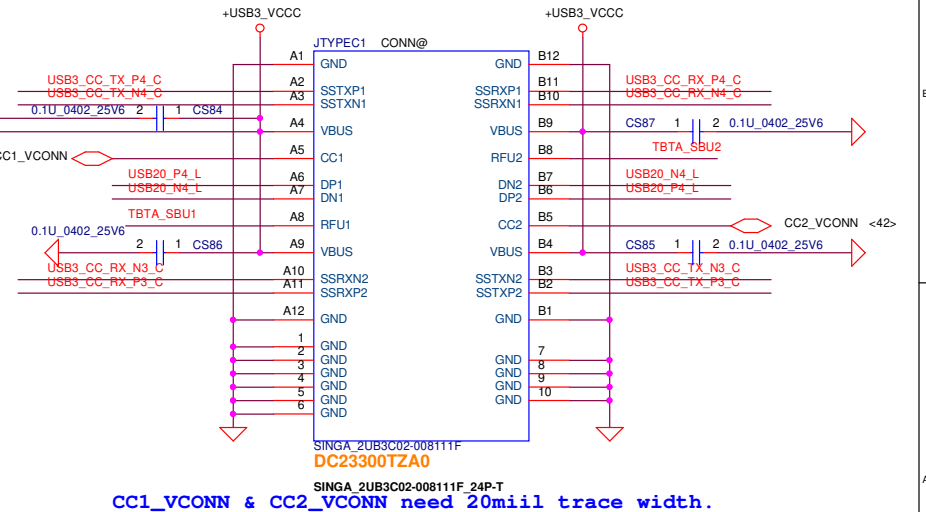
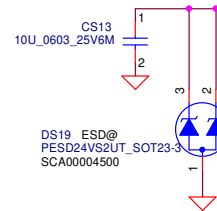
20191015 - Pin SWAP for layout
20191016 For ESD request - Gen2 Solution SC300006T00



G518 MOS Current Limit					
GPP B1 (TYPEC_1P5A)	GPP B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point	
L	L	6.2	0.9A	1.09A	
L	H	3.53	1.5A	1.92A	
H	L	2.54	2A	2.67A	
*H	H	1.94	3A	3.5A	



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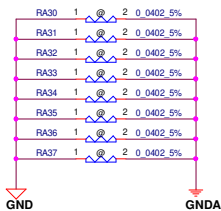
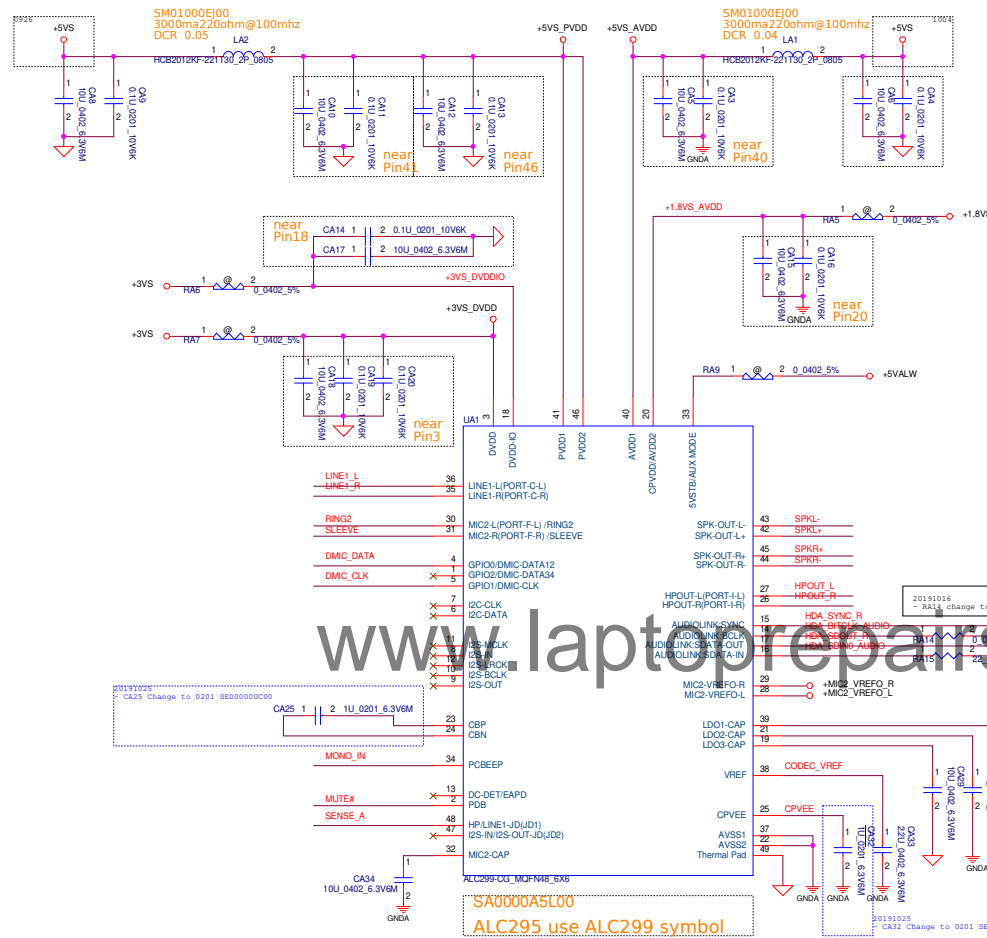


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				FH51MM/B LA-J871P	
				Date:	Tuesday, February 11, 2020
				Sheet	43 of 112

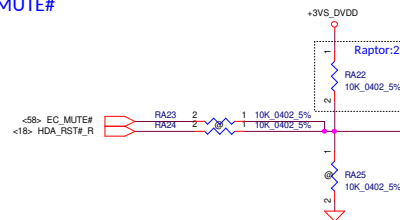
20190918

LAN more to IO/B
www.laptoprepairsecrets.com

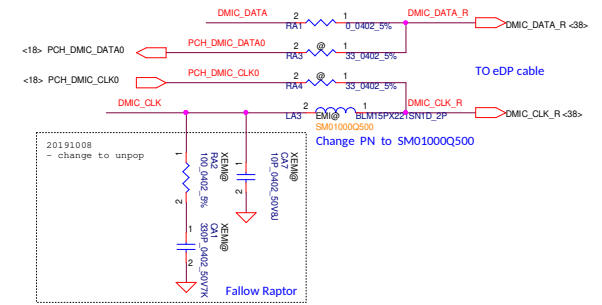
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title
				LAN Killer-E2600
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				FH51M M/B LA-J871P
				Date
				Tuesday, February 11, 2020
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				51 of 112
				Rev
				1.0



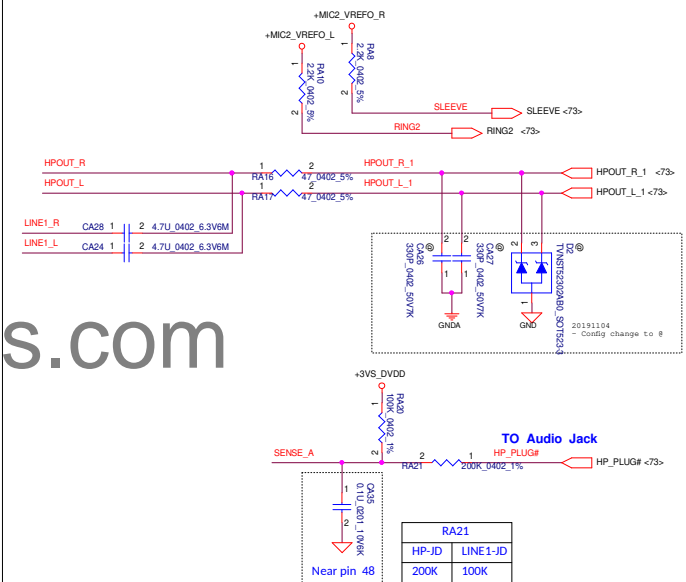
MUTE#



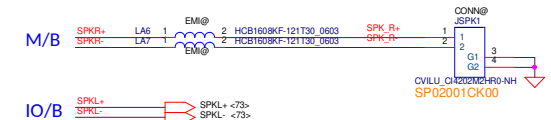
Digital MIC



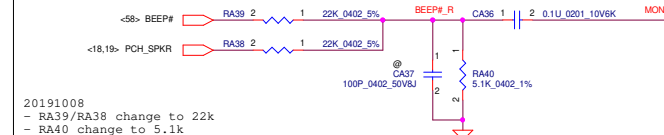
Headphone Out



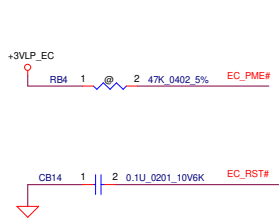
Speaker



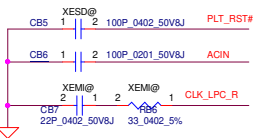
BEEP



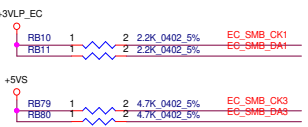
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For turn off internal LPC module of KB9032



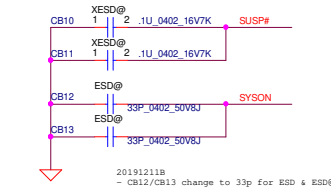
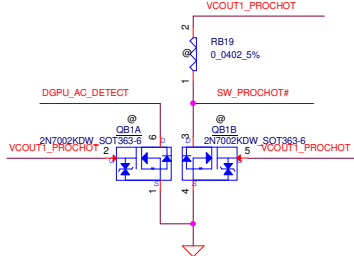
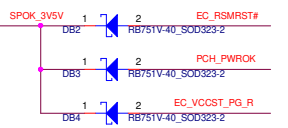
20200114 - CB5 Change to SE00000SE00 (0201)



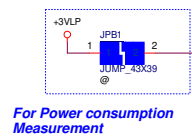
20191204 - RB79/RB80 change power source to +5VS for power leakage.



For abnormal shutdown

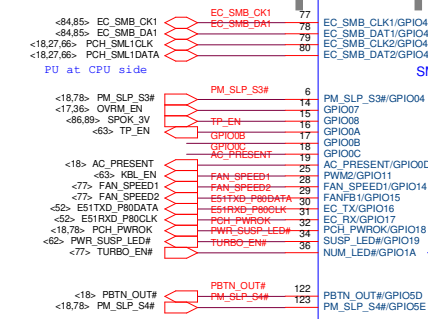
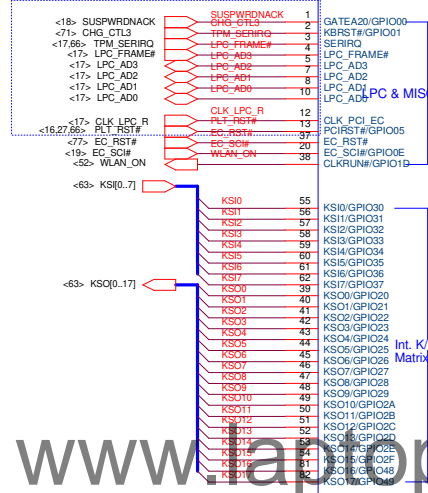


201912118 - CB12/CB13 change to 33p for ESD & ESD#



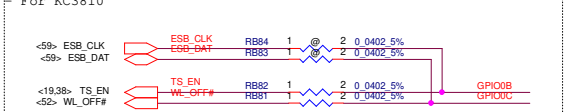
For Power consumption Measurement

ESPI Bus Pin : 1-5,7,8,10,12,14
LPC Bus Pin : 3-5,7,8,10,12,13

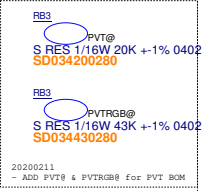
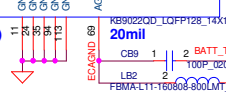


CO-LAY with KB9032QA (SA000080J00)

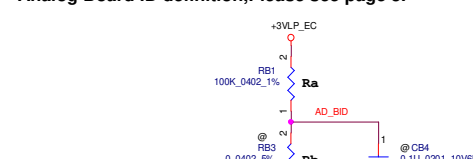
20191008 - For KC3810



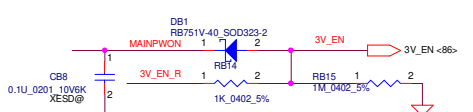
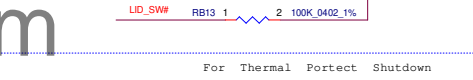
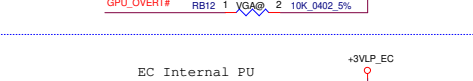
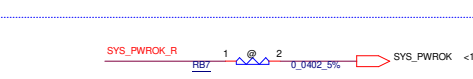
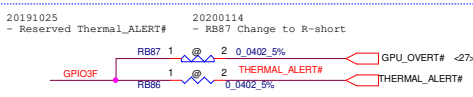
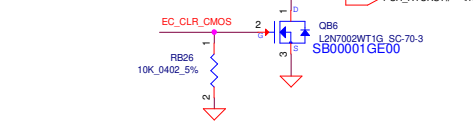
2015/1/9 acer require: reserved protect circuit when adaptor 107% happen



Board ID - Analog Board ID definition, Please see page 3.



near SOC



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Size		E C E NE-KB9022	
Custom		FH51M M/B LA-J871P	
Date:		Tuesday, February 11, 2020	
Sheet		58 of 112	

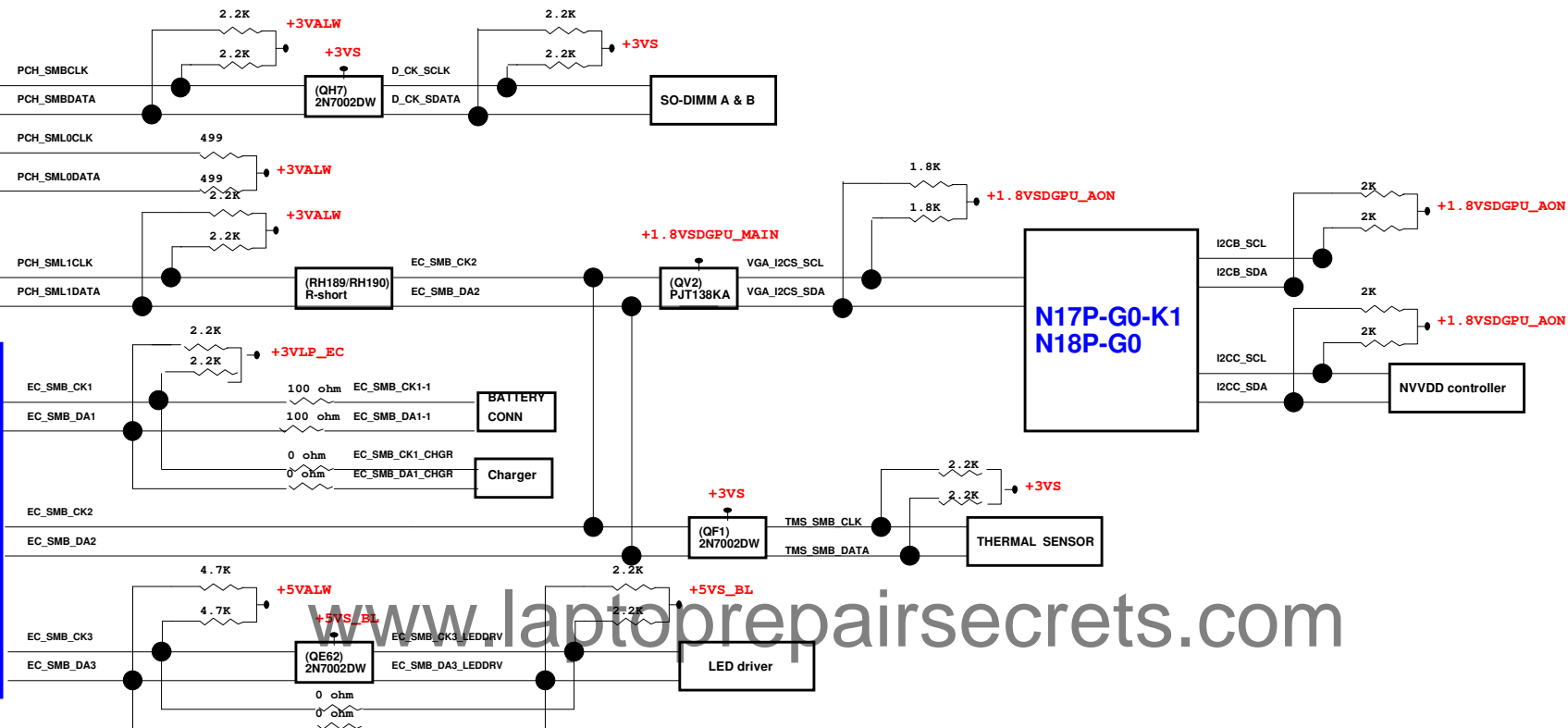
OMEN New ESB CLK&DAT for Extend I/O



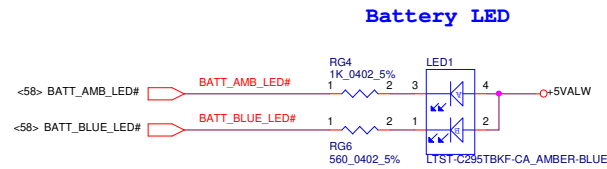
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Cannonlake
PCH - H

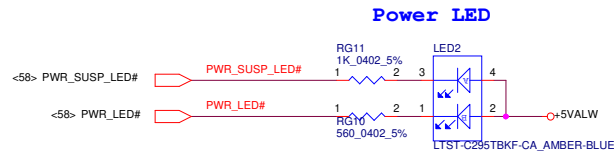
KB9022



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20200211
- RG4/RG11 change to 1k



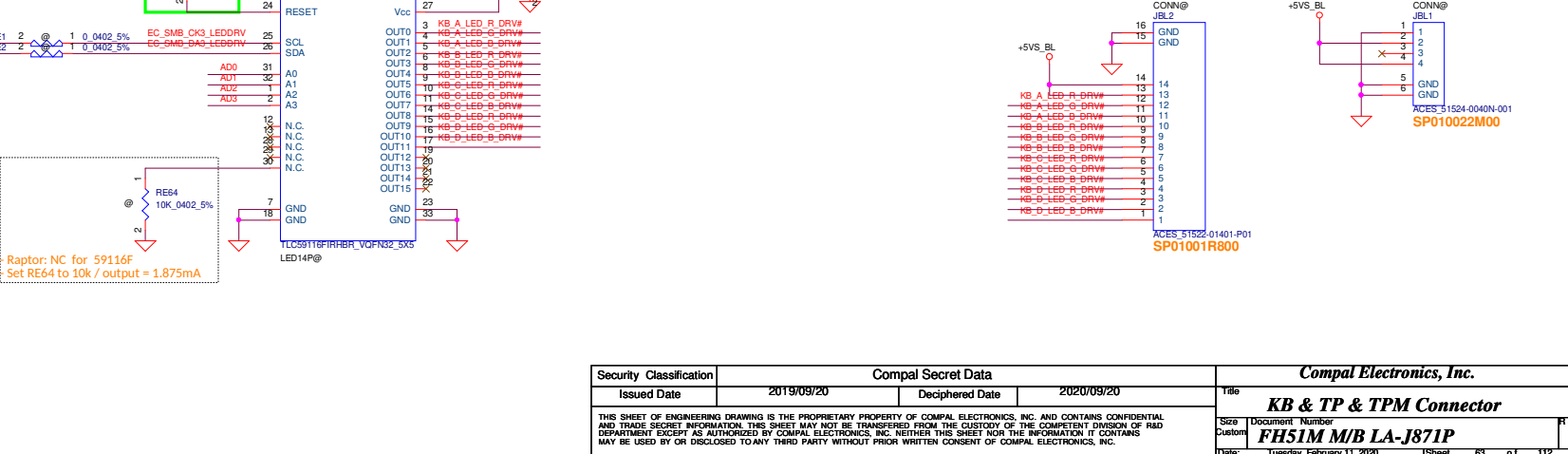
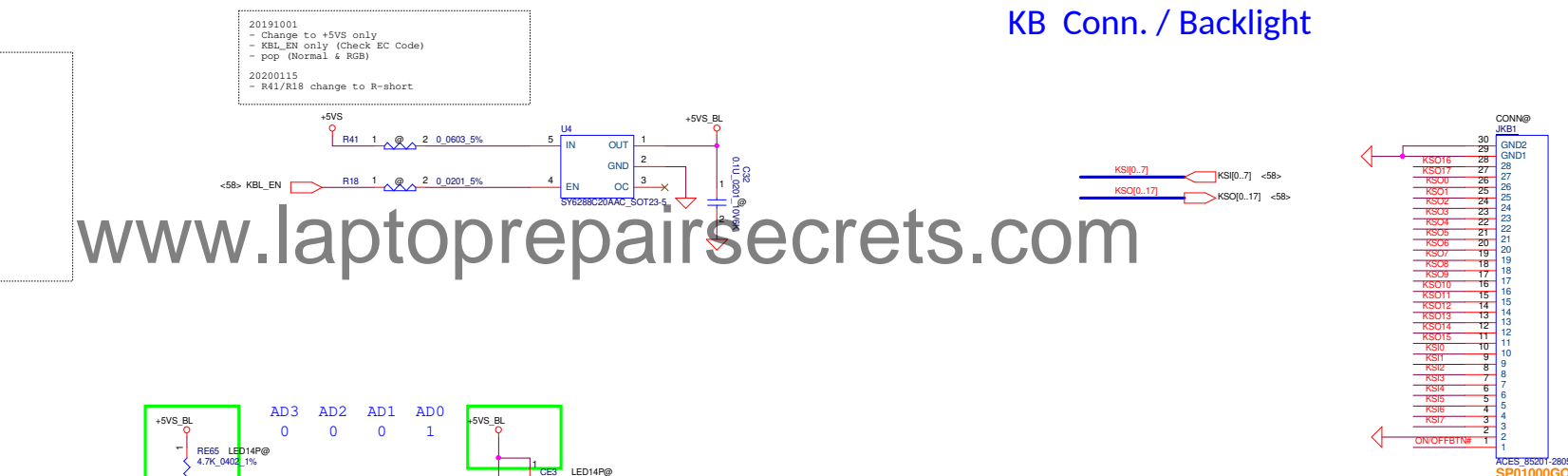
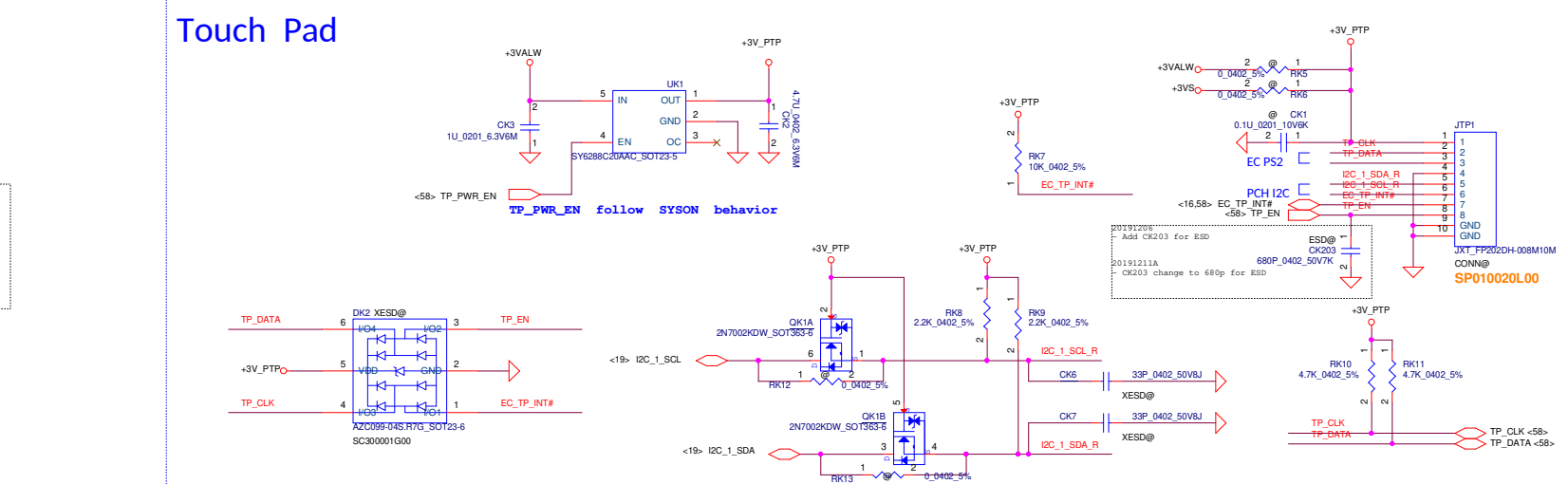
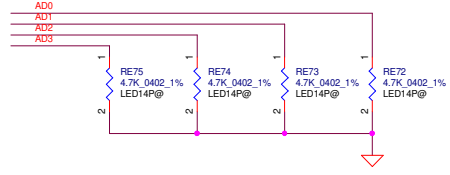
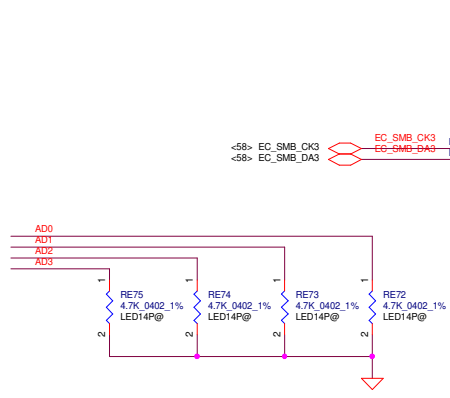
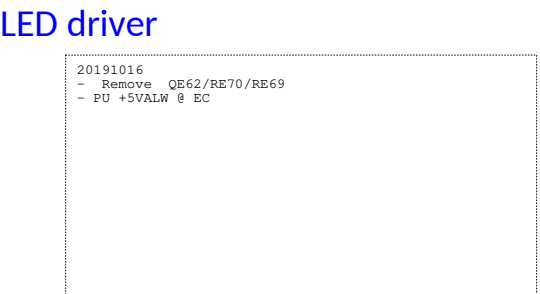
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				Sheet	82 of 112

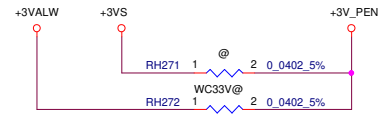
ON/OFF BTN
- For TEST

LED driver

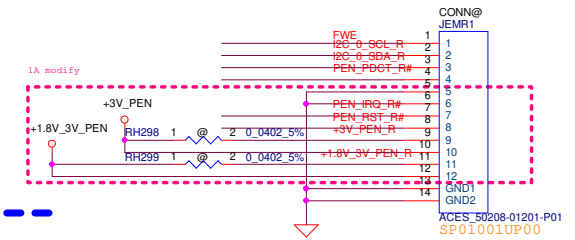
Touch Pad



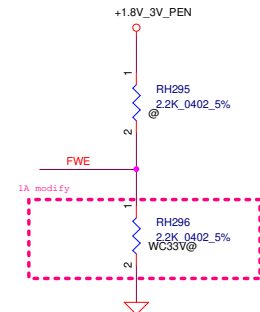
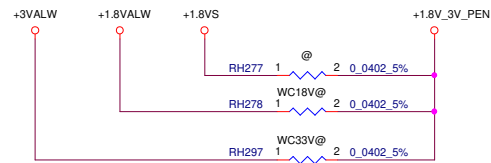
3V_PEN



EMR



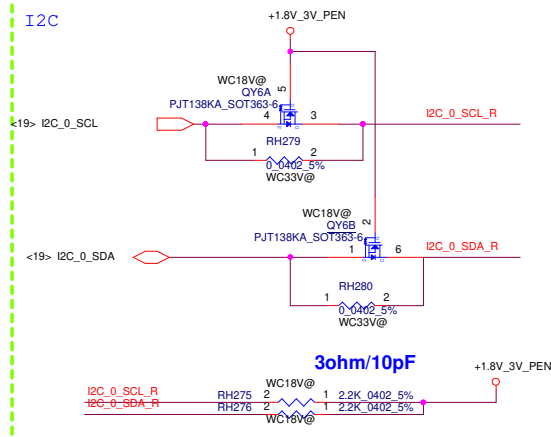
1.8V_PEN



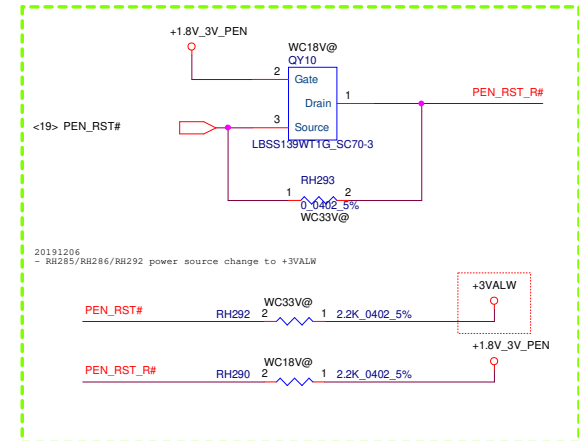
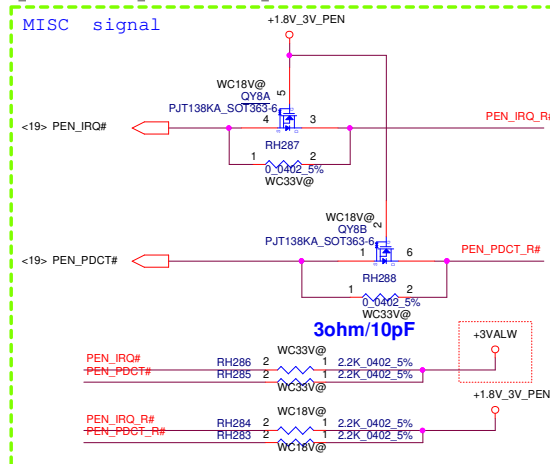
20191008
- QY6/QY8 change to SB000016K00
Default use 0ohm(WC33V@)

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I2C

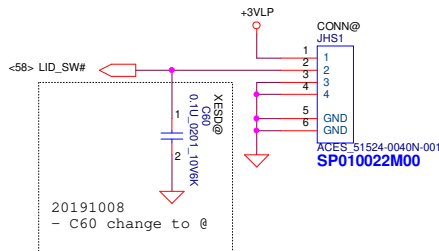


MISC signal

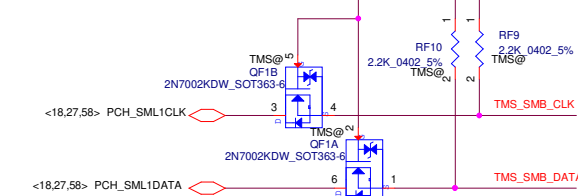


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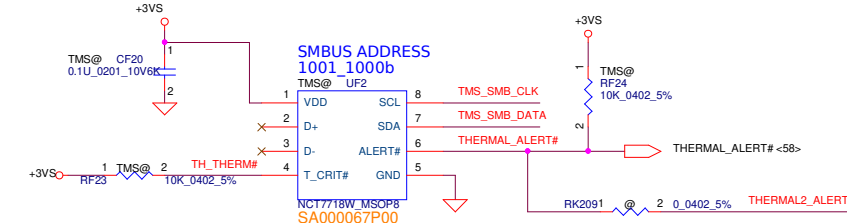
To Hall sensor/B



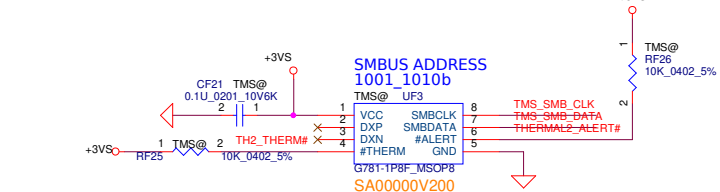
THERMAL SENSOR



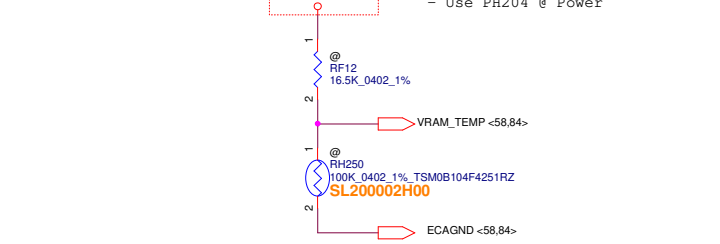
Close to SO-DIMM



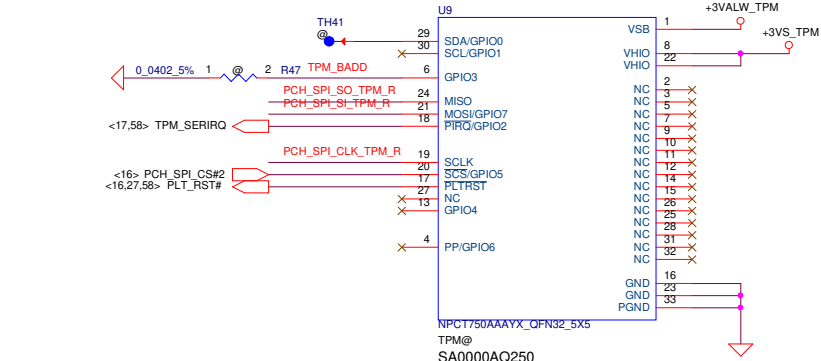
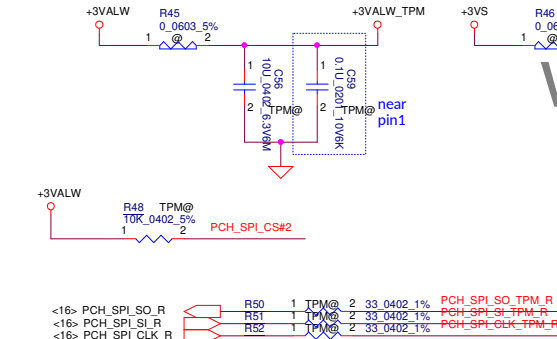
Close to Thermal SKIN



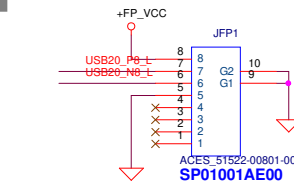
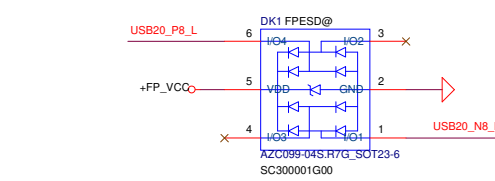
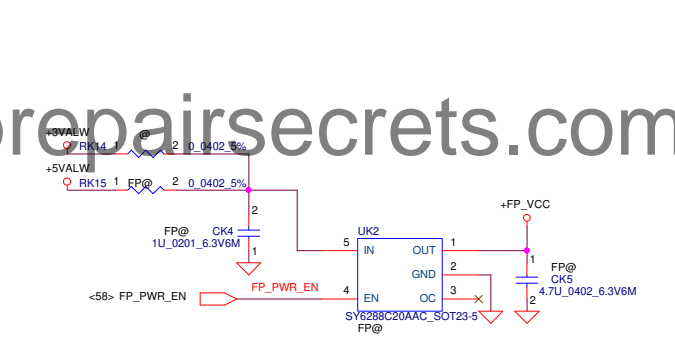
Close to VRAM choke



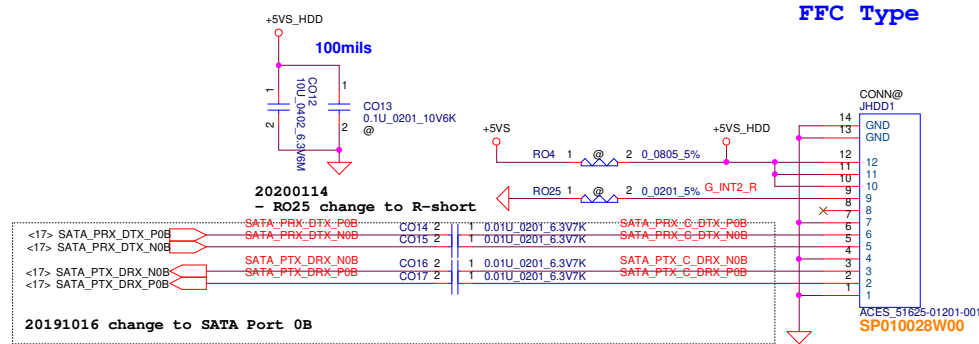
TPM



Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC



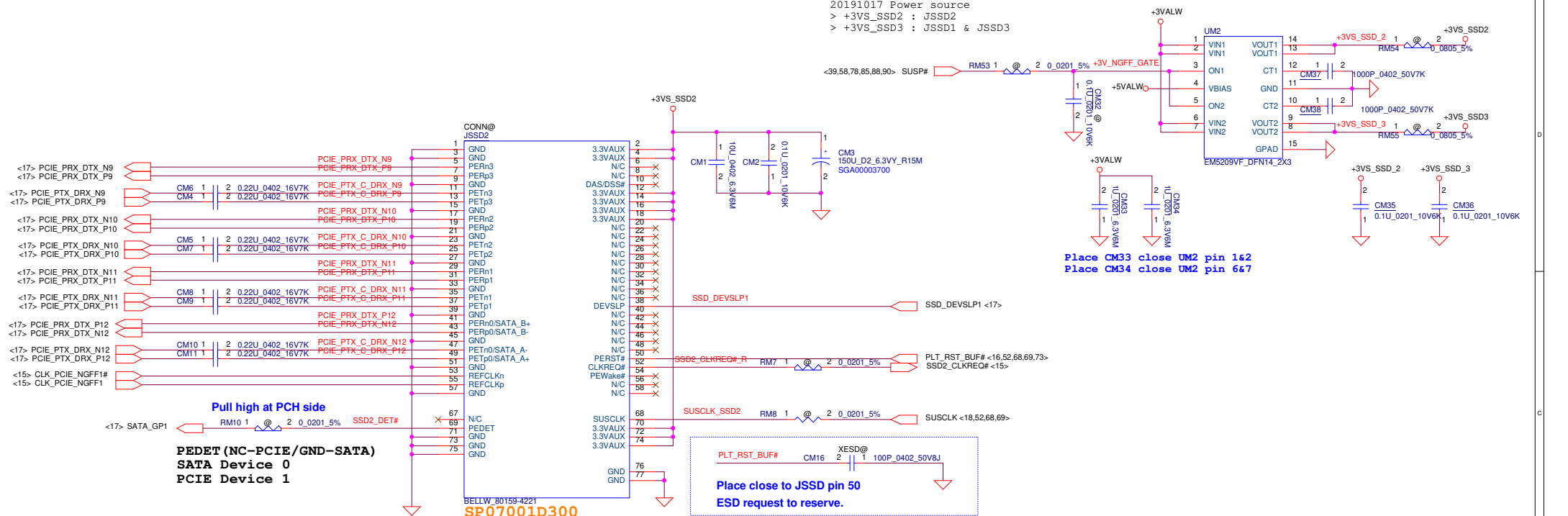
www.laptoprepairsecrets.com

20190918

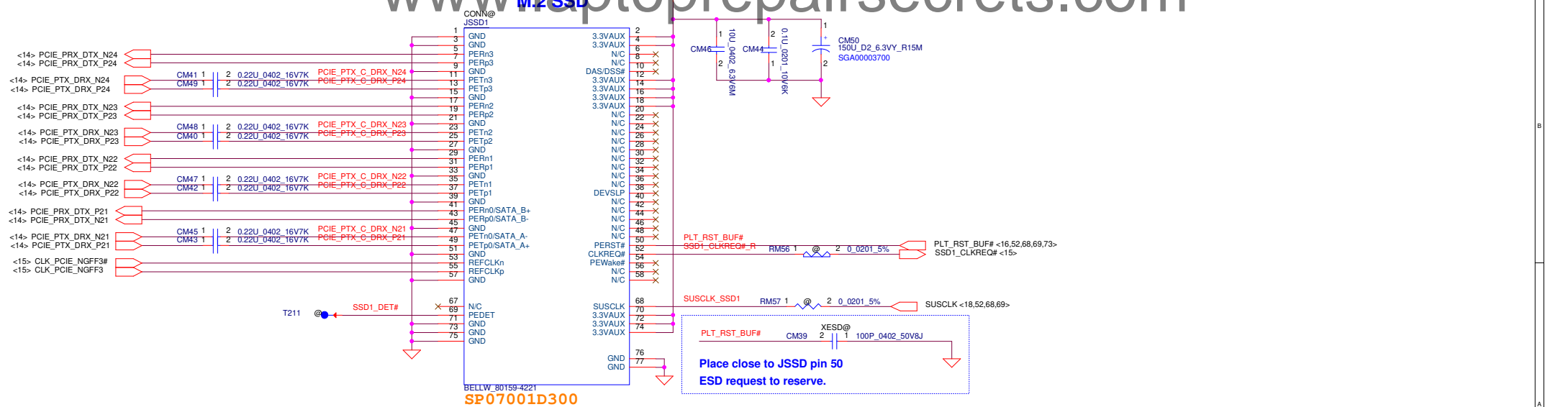
Remove HDD Re-driver

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				Size Custom	Document Number FH51M M/B LA-J871P
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20191017 Power source
> +3VS_SSD2 : JSSD2
> +3VS_SSD3 : JSSD1 & JSSD3

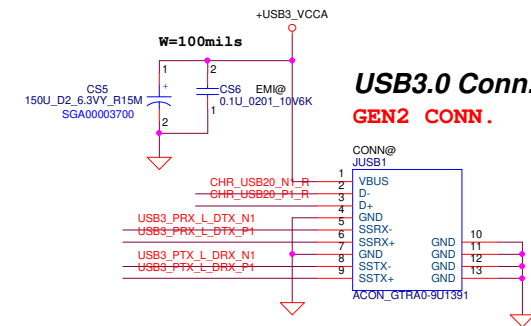
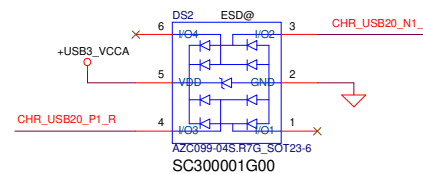
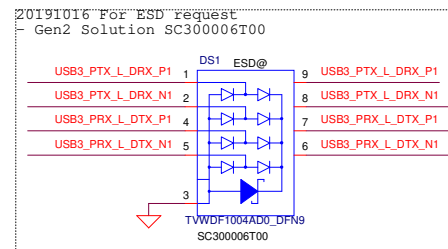
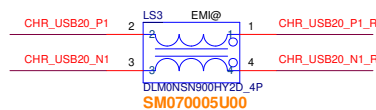
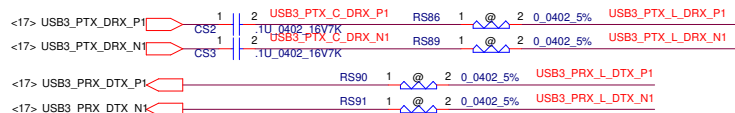


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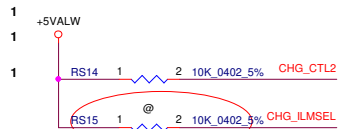


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Size	Document	Number	Rev	Date	
Custion		FHS1M M/B LA-J871P	1.0	Tuesday, February 11, 2020	
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USB3.0



USB Host Charger

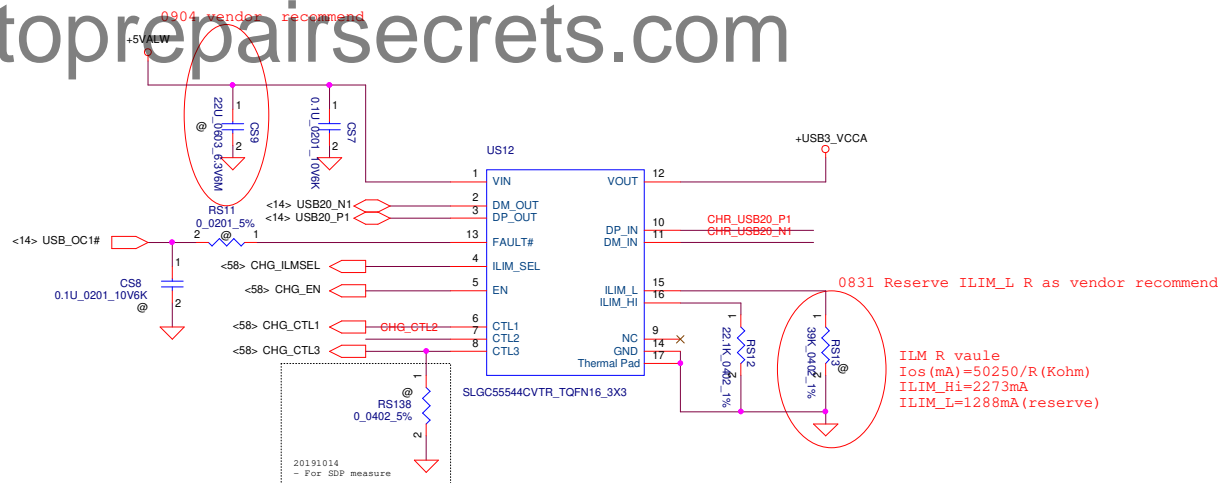


0911 Reserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	1	0	1	1	SDP1-OFF	ILIM_H		Port power off
0	1	0	1	1	SDP1	ILIM_H		Data Lines Connected
0	1	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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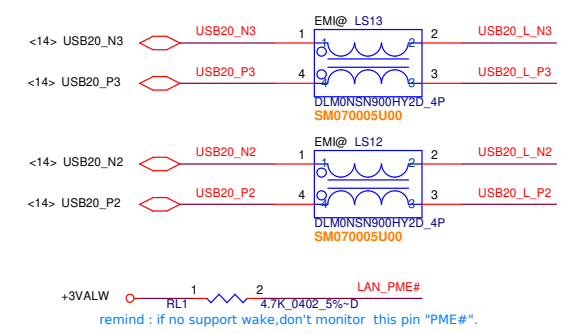
20190918

USB3 Port3 move to IO/B

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IO/B CONN



I209A
- IO_B change pin define

20191008
- LAN_PCIE&CLK Remove AC Cap > Vender confirm
(CL136/137/138/139)

20191016
- Change to Port5

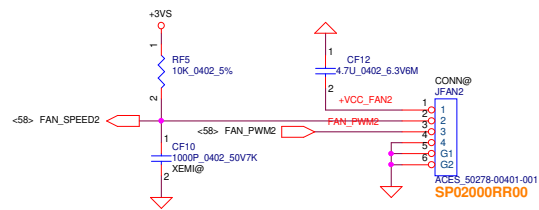
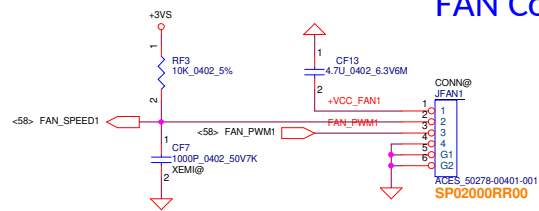
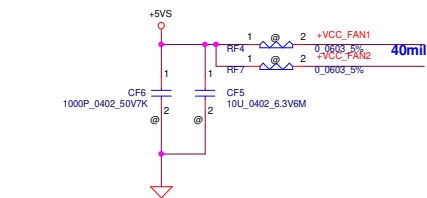
20191008
- LAN_PCIE&CLK Remove AC Cap > Vender confirm
(CL136/137/138/139)

20191023
- Add +3VS

20191023
- Add +3VS

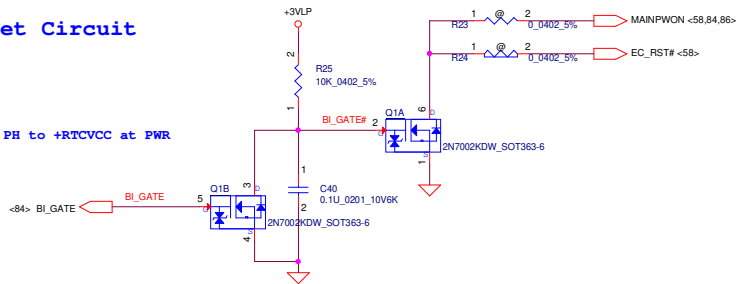
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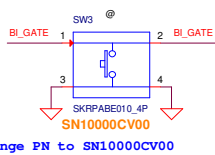


Reset Circuit

BI_GATE PH to +RTCVCC at PWR side

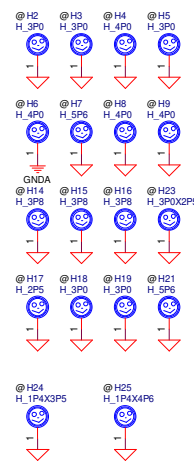


Reset Button



change PN to SN10000CV00

Screw Hole

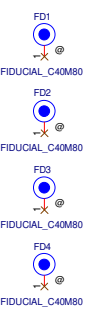
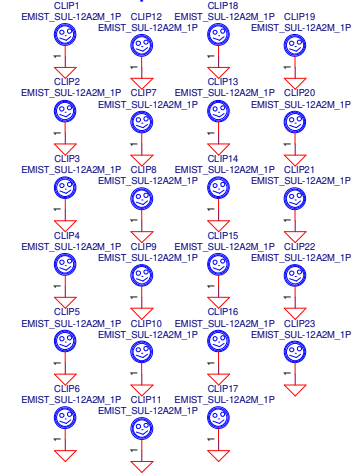


2019I210B
- H6 change to GND for Layout

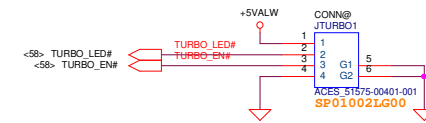
Stand OFF



Clips



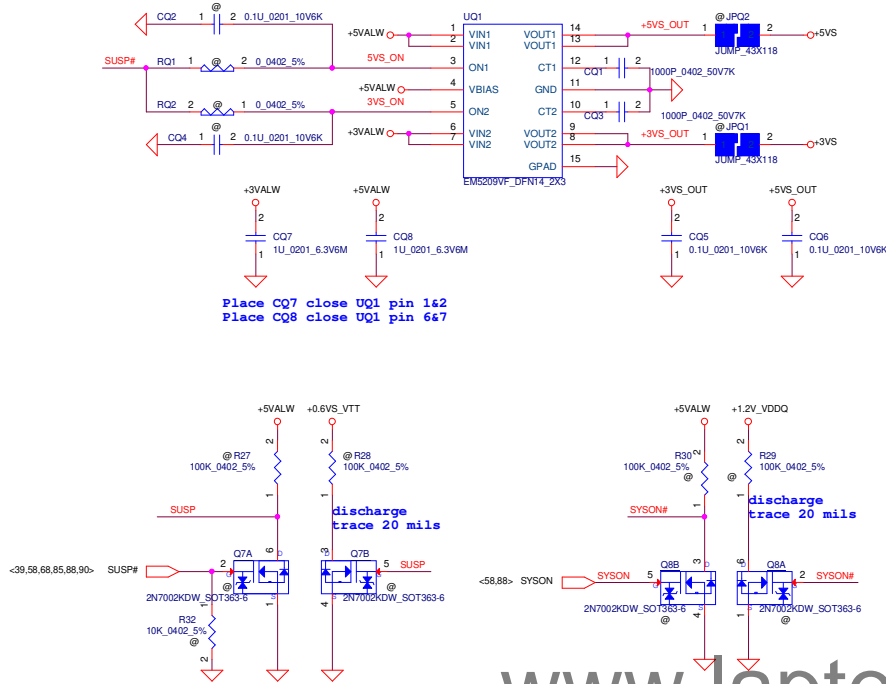
Turbo Key



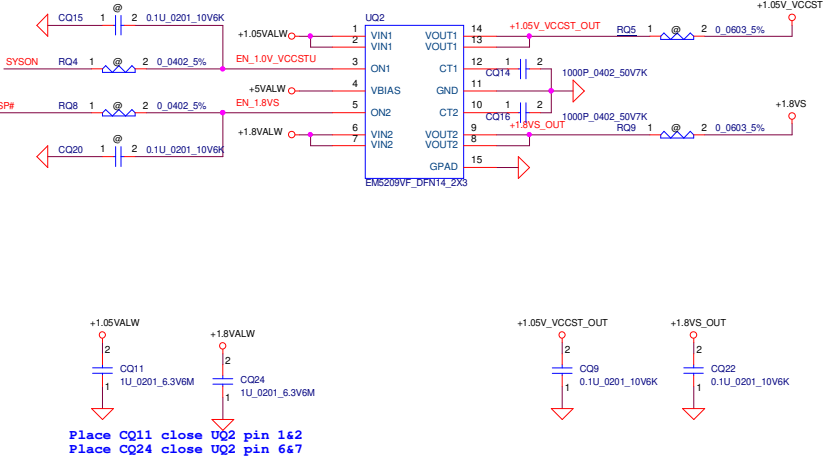
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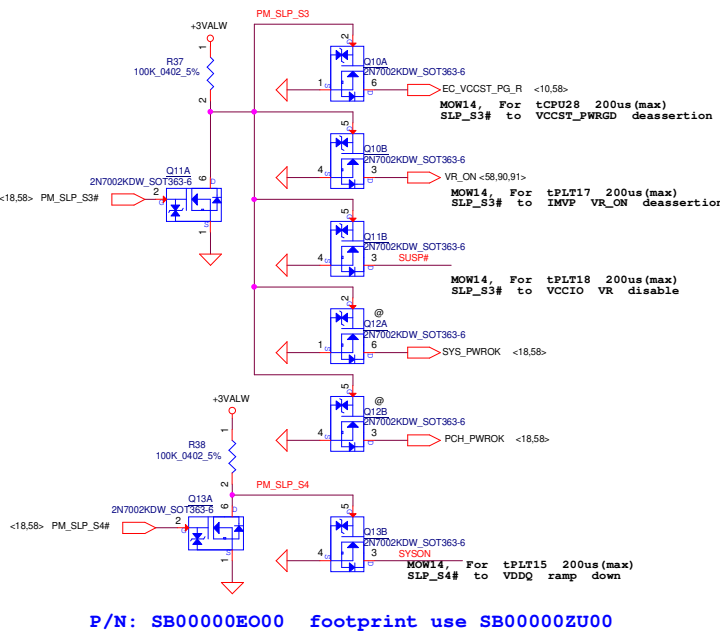
System DC interface



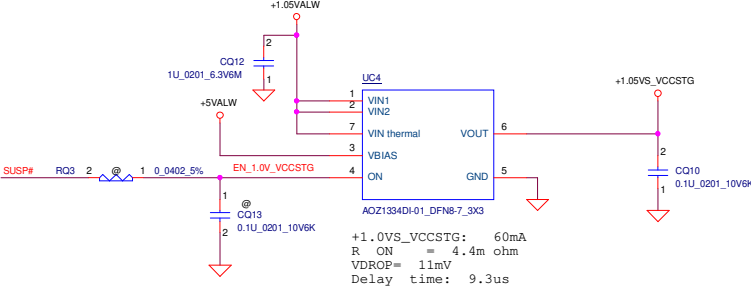
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



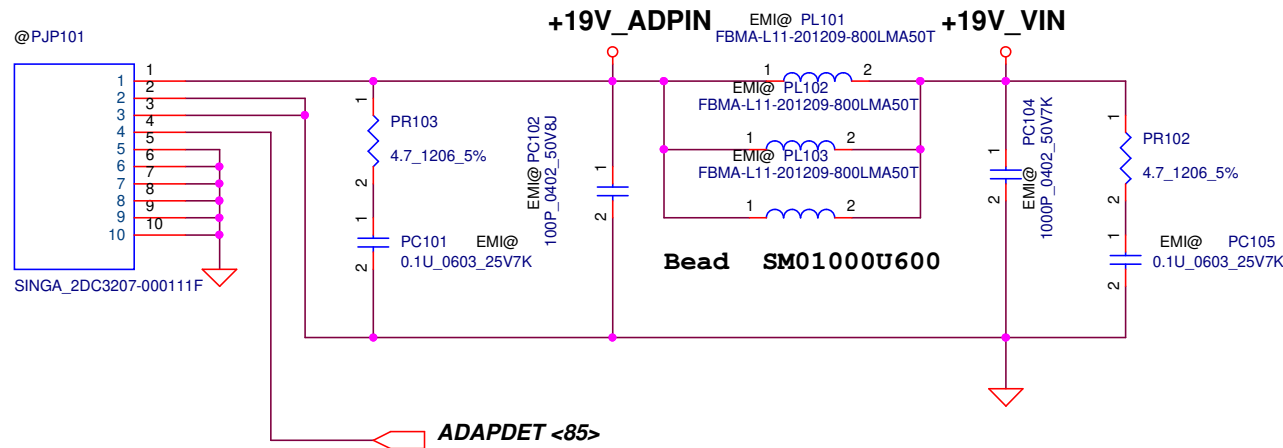
For Power ON/Off Sequence



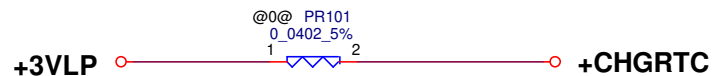
+1.05VALW TO +1.05VS_VCCSTG



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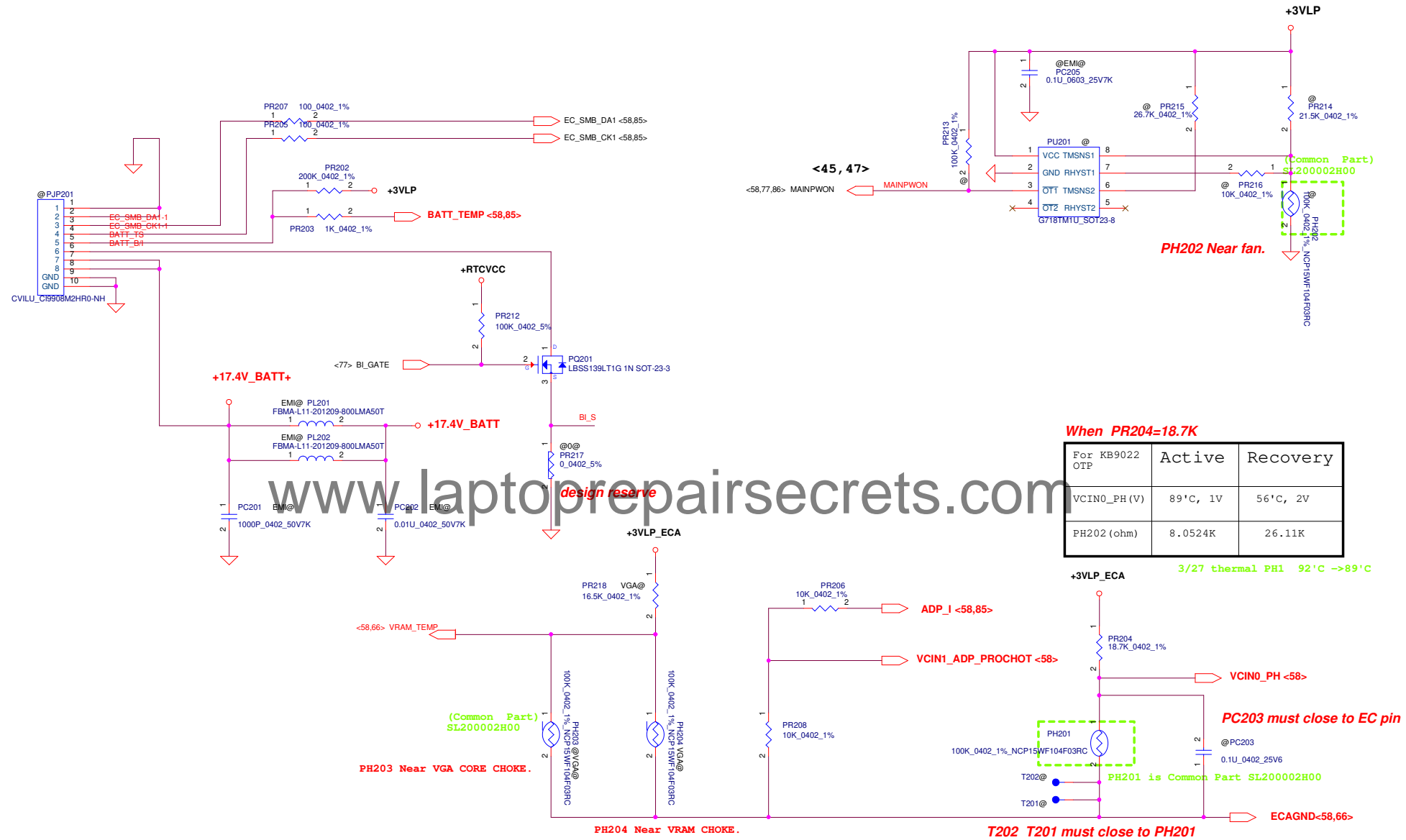
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Battery Bot Side

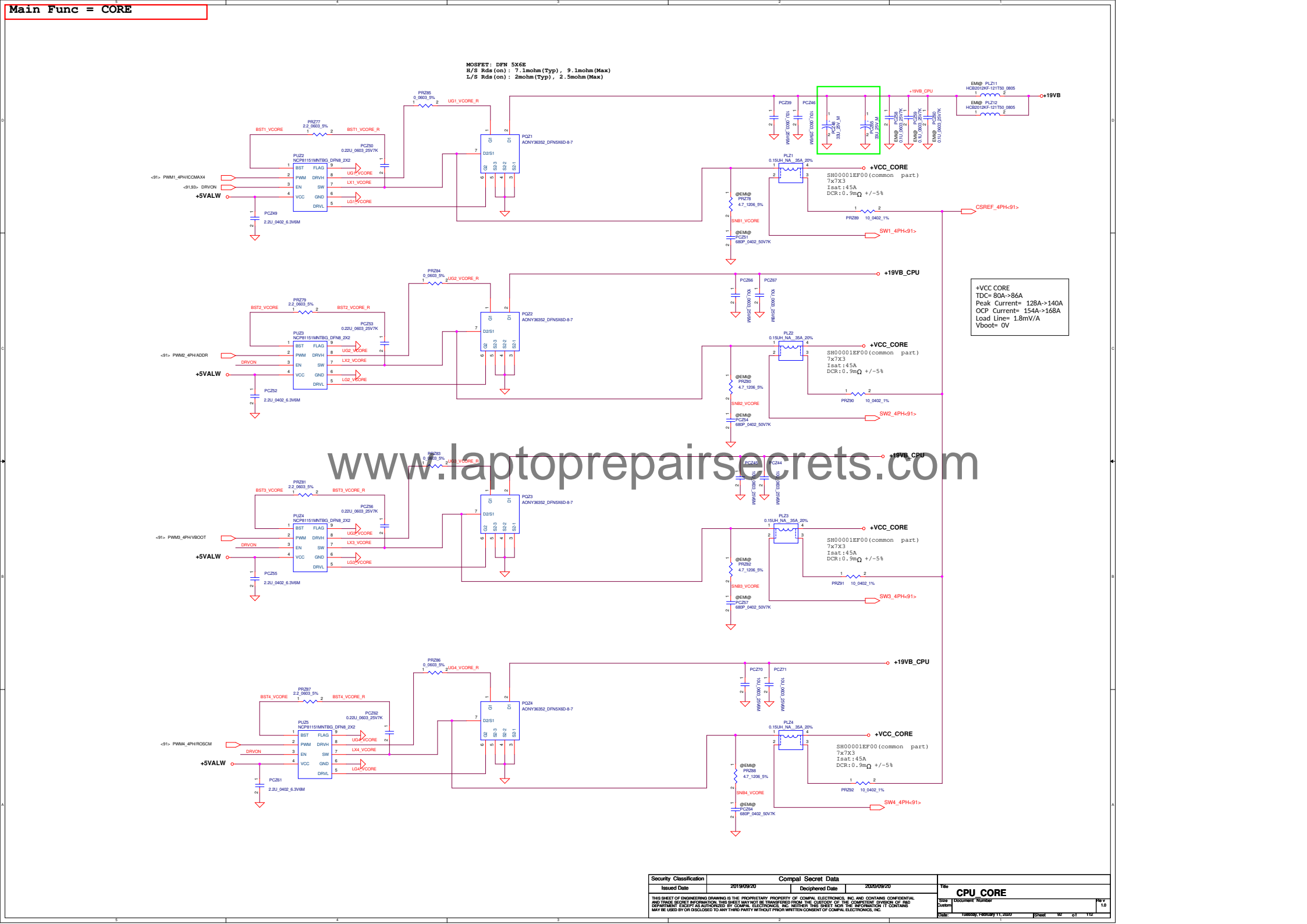
- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TEMP
- PIN6 BI
- PIN7 Batt+
- PIN8 Batt+



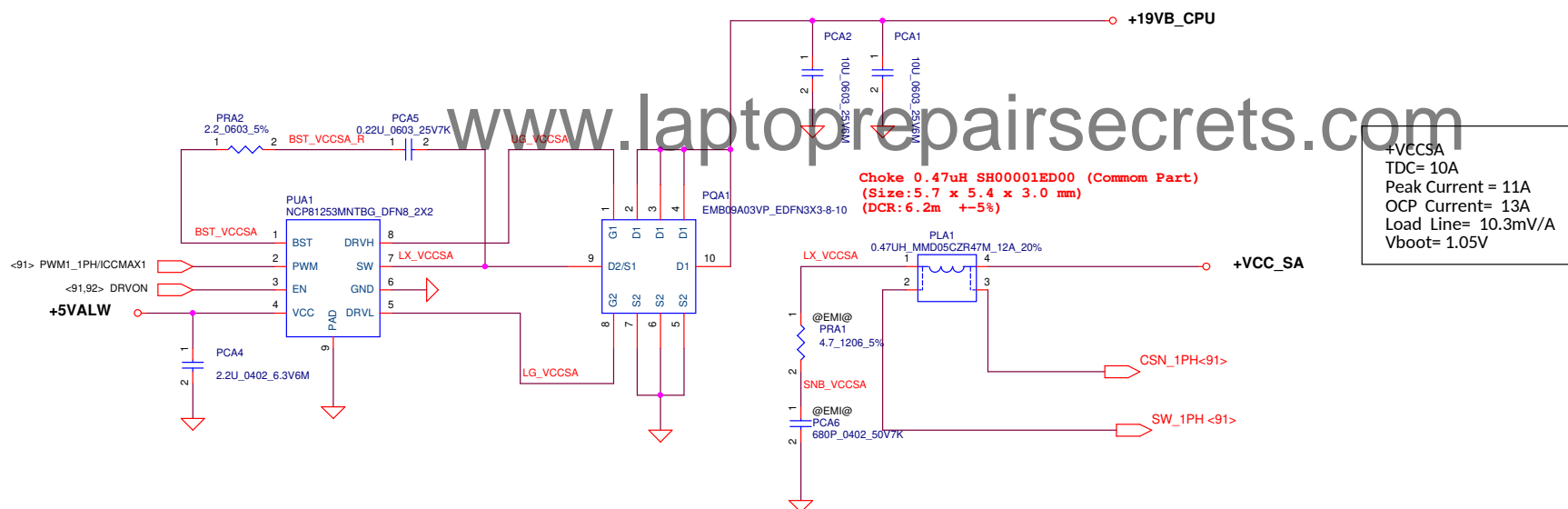
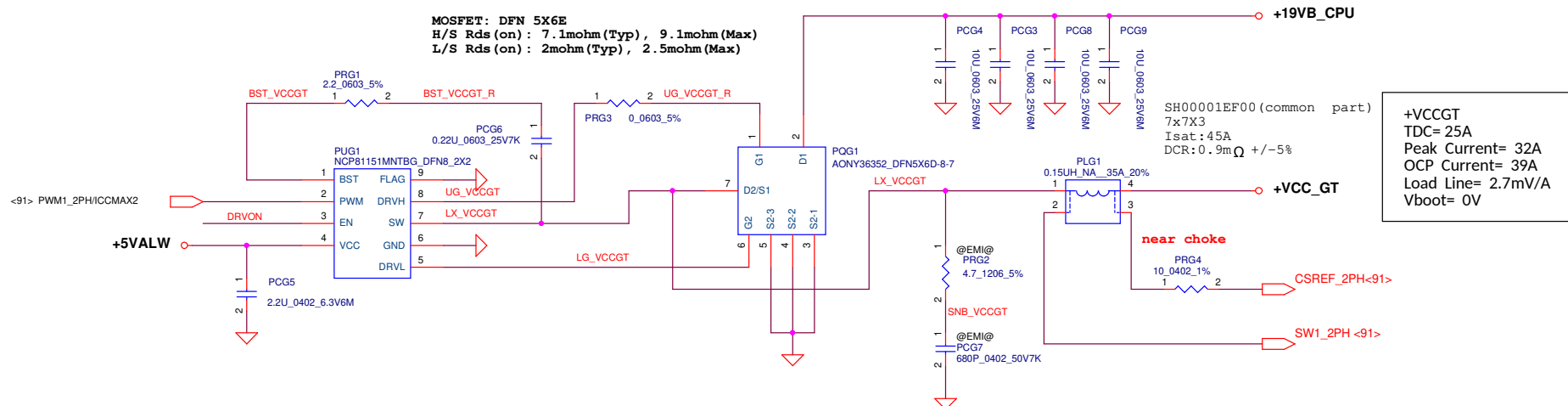
When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89'C, 1V	56'C, 2V
PH202 (ohm)	8.0524K	26.11K

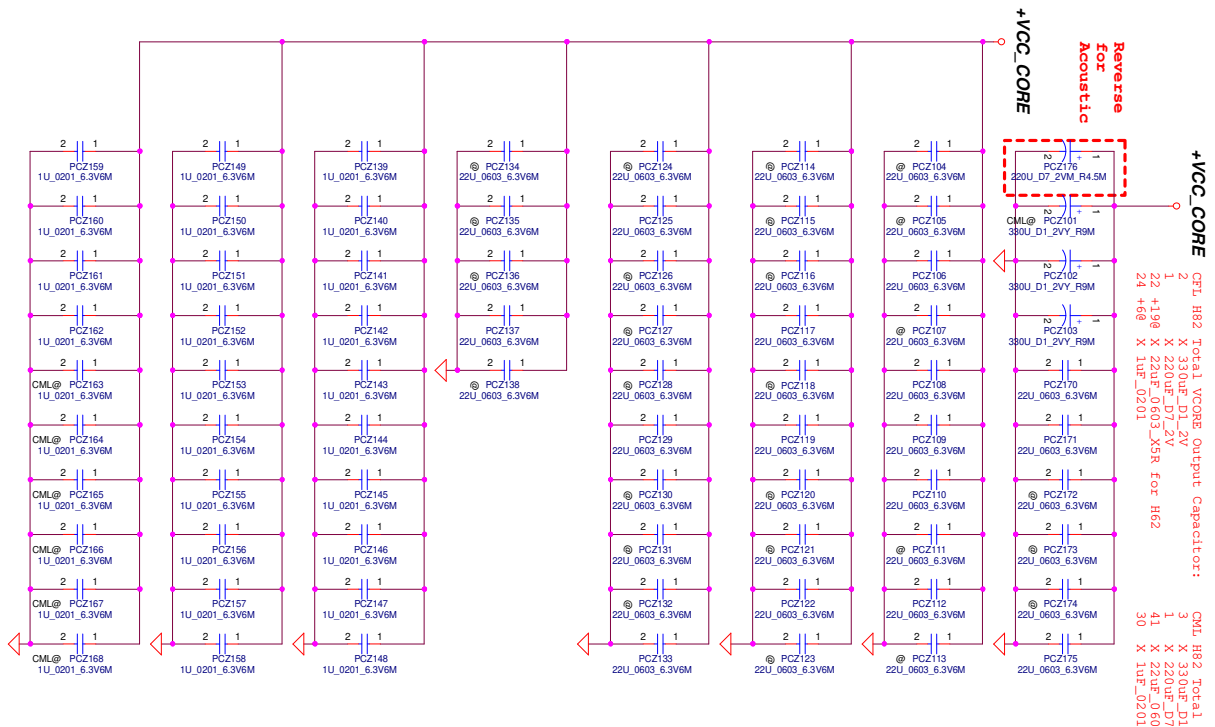
$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$



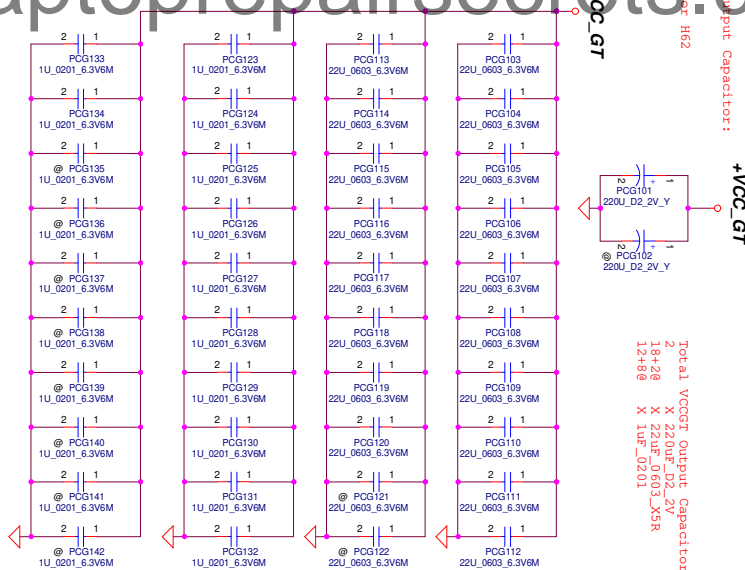
Main Func = VCCGT/+VCCSA



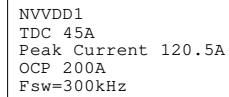
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title +VCC_GT+VCC_SA			
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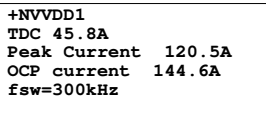
PWR_VGA_UP9512P

FXXXX M/B LA-1871P

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PWR_+NVVDDM

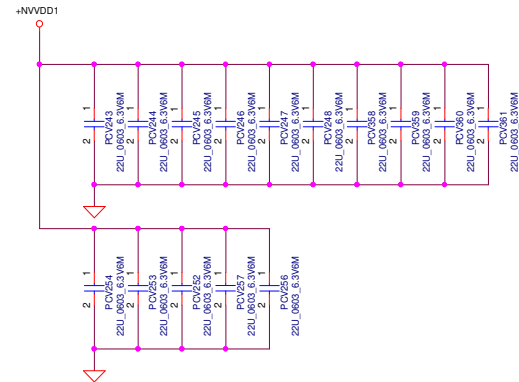
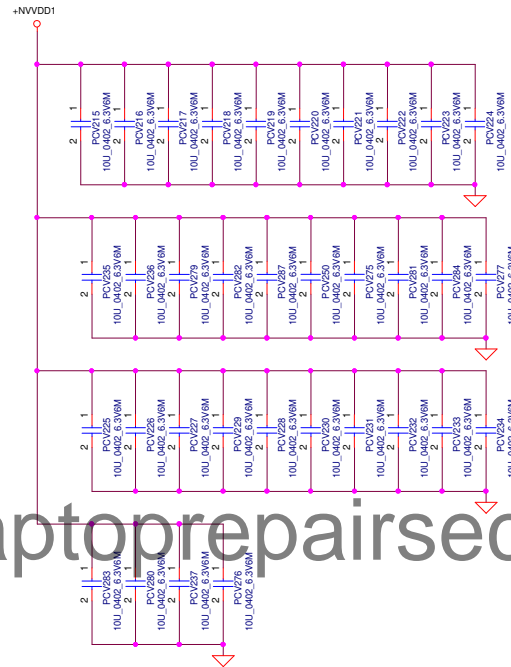
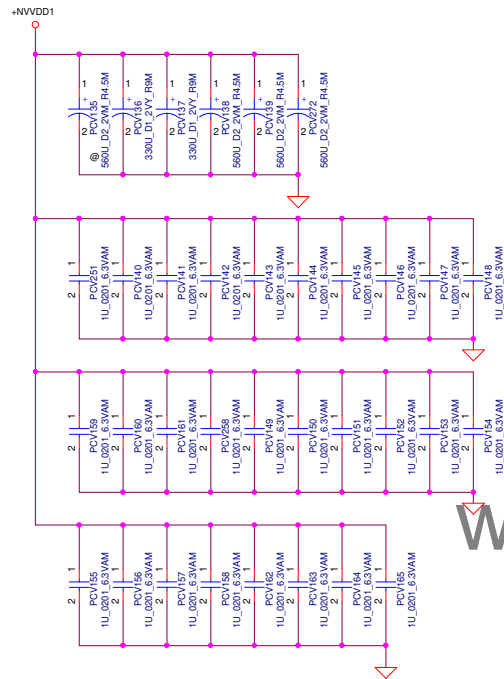
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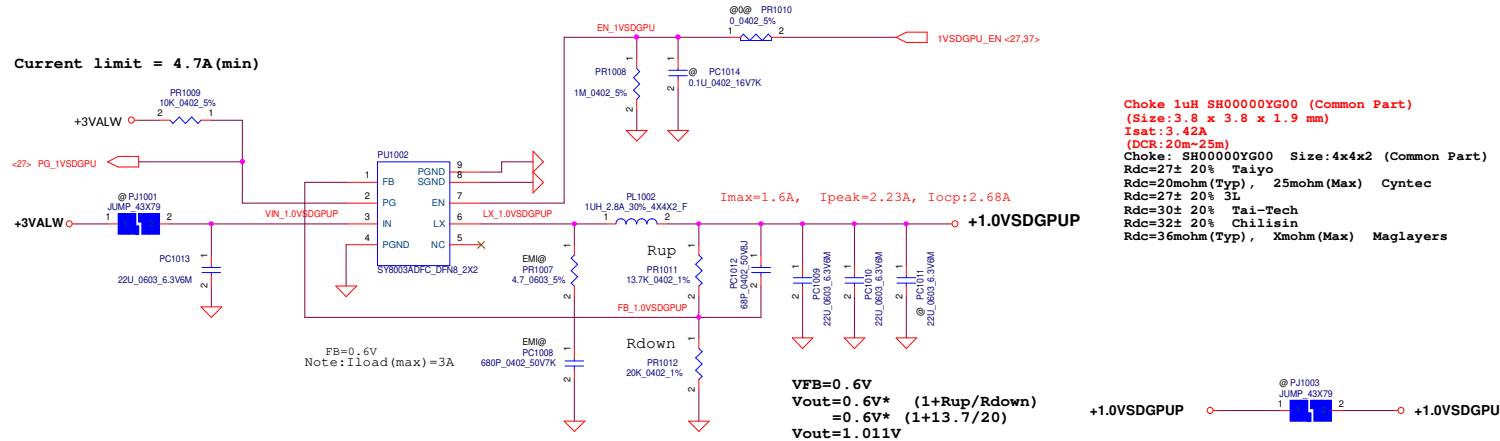
N18P-G62
+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X65) 23 X 10uF (0603 X65) 4 X 22uF (0805 X65) 3 X 47uF (0805 X65)	2 X 470uF (Poscap)
FBVDDQ (GPU side) ¹		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X65) 5 X 10uF (0603 X65)	7 X 10uF (0603 X65) 9 X 22uF (0603 X65)



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[illegible]

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Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	52	CNVA	1209B	CNVA-Intel review (J945V9)	Add R3M67 / R3M68 0-ohm Add P4U R3M70 / PD R3M69 (Reserve)		
2	52	ELABRT_BFI	1209B	ELABRT_BFI review	R3M66 Change to @ for Vender review		
3	81-111	POWER_SCH	1206A	POWER_update	Combined Power SCH (1204)		
4	40	PDMMI	1206B	PDMMI EMI solution	Remove R352/R353/C327, L315 change to pop (EMI@).		
5	17/69	SSD3	1206B	SSD3 SATA/PCIE detect	SATAGP change to GP4 & R3H303 PFI		
6	64	EMR	1206B	EMR Power source	R3H285/R3H286/R3H292 power source change to +3V3/LW		
7	63	Touch Pad	1206B	ESD	Add C3303(100p) for ESD		
8	27	VGA	1206C	CLAREEQ	R3R83 change to pop(VGA@)/ C3V226 change to unpop (@)		
9	19	PROTECT PD	1206C	PROTECT PD	defined as Protect - 50 (PD1:H / PD0:L)		
10	38	Panel OD	1206C	Panel OD function	R3X11 change to unpop & BICAS needs to detect panel to select H or L .		
11	16/58	BFI_CN	1206C	BFI_CN change to PCH	R3H304 pop (PFI) & R3B85 unpop (EC)		
12	73	IO_B conn.	1209A	IO_B conn.	IO_B change pin define		
13	15/68/69	M2 SSD	1209B	Fixed naming	> SSD1 - GPP_B9/CLAREEQ4# (PCPE only) (2018 @SSD2) > SSD2 - GPP_B8/CLAREEQ3# (PCPE/SATA) (2018 @SSD1) > SSD3 - GPP_B10/CLAREEQ5# (PCPE/SATA) (2019 REV)		
14	52	CNVA	1209B	CNVA-Intel review (J945V9)	R3M70 change power source to +3V3_WL3N		
15	81-111	POWER_SCH	1209C	POWER_update	Combined Power SCH (1209)		
16	81-111	POWER_SCH	1210A	POWER_update	Combined Power SCH (1209B)		
17	77	H6	1210B	For Layout	H6 change to G3D3A for Layout .		
18	69	SSD3	1210B	BCM Config	ADD SSD3@ for BCM		
19	58	Board PD	1210B	Board PD config	ADD PPI1@ & PPIPRGB@ for PPI BCM		
20	52	CNVA	1210C	CNVA-Intel review (J9451M)	> R3M69 change to 71.5k & CNV1@ > R3M70 set CNV1@ > R3H22 change to 20K > R3M36/R3M37/R3M67/R3M68 change to 22 ohm		
21	63	ESD	1211B		> Pop C3303 680p & ESD@ > CB12/CB13 change to 33p for ESD & ESD@		
				PPI Rev 1.0			
22	63	SW	0114A	BFI	SW1 set E-VI@		
23	58		0114A	Action plan	C36/C39 100P 0402 Change to SE00000SE00 (0201)		
24	15		0114A	Action plan	C37/C38 10P 0402 Change to SE173100780 (0201)		
25			0114A	Action plan	R3Q25 Change to 0201 R_short		
26			0114A	Action plan	R3H100 Change to 0603 R_short		
27			0114A	Action plan	R3T10/R3G137/R3G9/20R87/R3X8/R3X9 Change to 0402 R_short		
28	52	CNVA	0114A	CNVA-Intel review (J945V9)	Add C3451/CB152/10K Add C3453/CM54 0.01u		
29	81-111	POWER_SCH	0114B	POWER_update	Combined Power SCH (0114B)		
30	63		0119B	Action plan	R3I1 Change to 0603 R_short R3I8 Change to 0201 R_short *remove R3BLED@		
31	81-111	POWER_SCH	0116A	POWER_update	Combined Power SCH (0116)		
32	6	CFU/PCU	0211A		Update CFU/PCU PFI & config		
33	62	LED	0211A		R3G4/R3G11 change to 1k		
34	58	Board PD	0211A	Board PD config	ADD PPI1@ & PPIPRGB@ for PPI BCM		

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